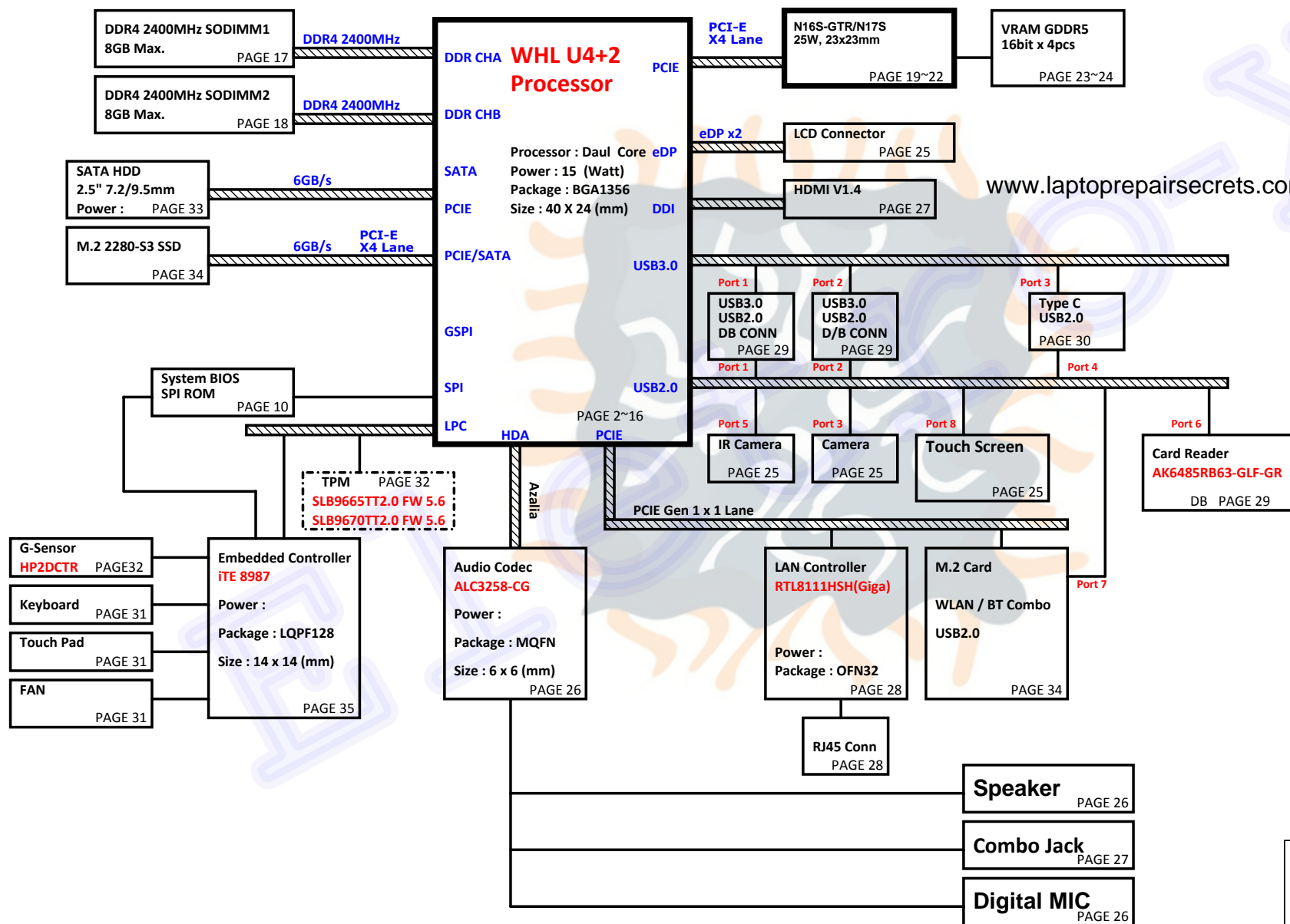
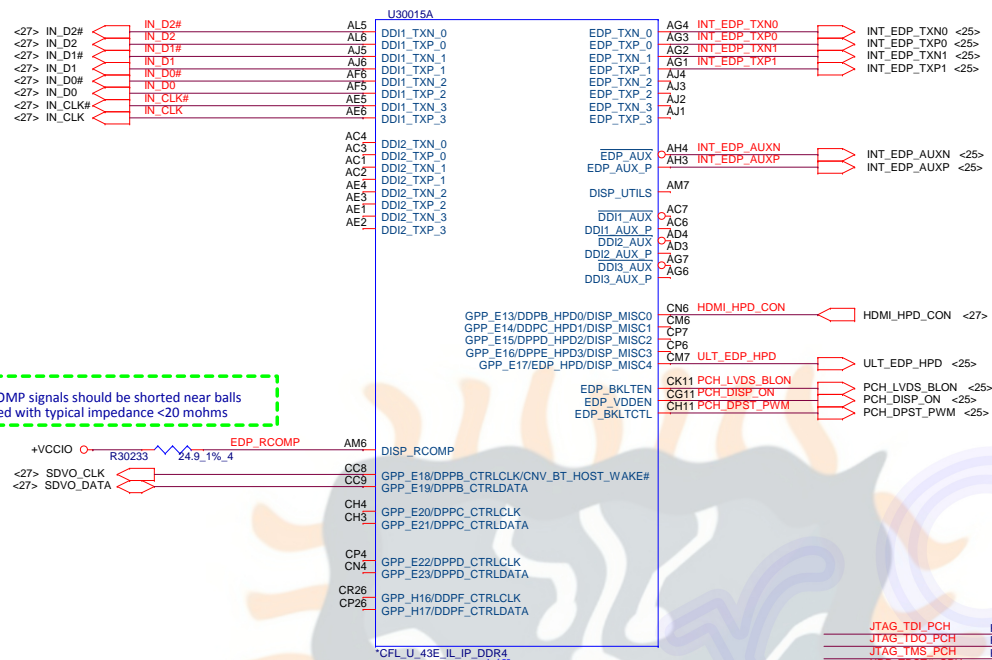


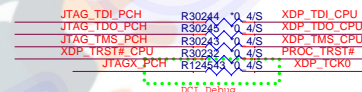
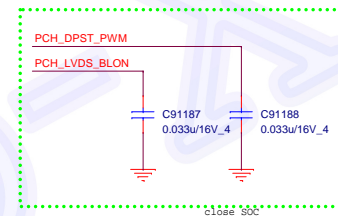
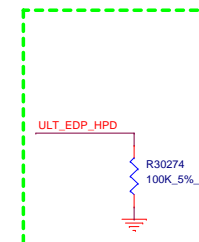
LAYER 1 : TOP  
LAYER 2 : SGND  
LAYER 3 : IN1  
LAYER 4 : IN2  
LAYER 5 : SVCC  
LAYER 6 : IN3  
LAYER 7 : SGND  
LAYER 8 : BOT



## HDMI



Reserve EDP\_HPD opposites circuit!

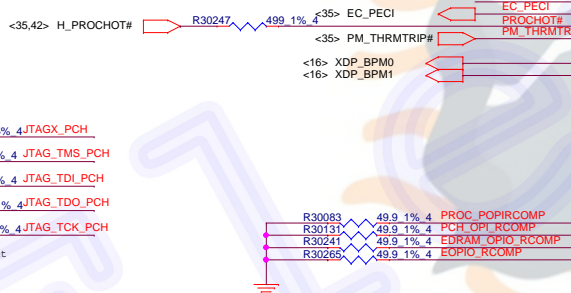
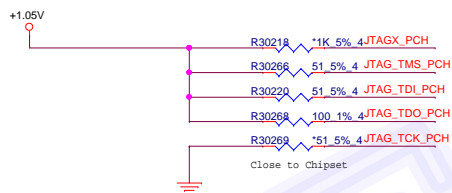
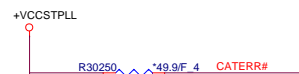
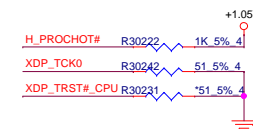
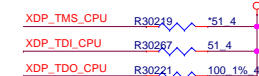


Close to EC

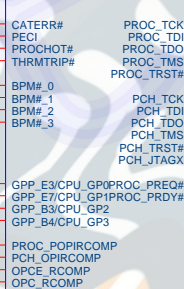


Processor pull-up (CPU)

PLACE NEAR CPU



U30015D



4 of 20

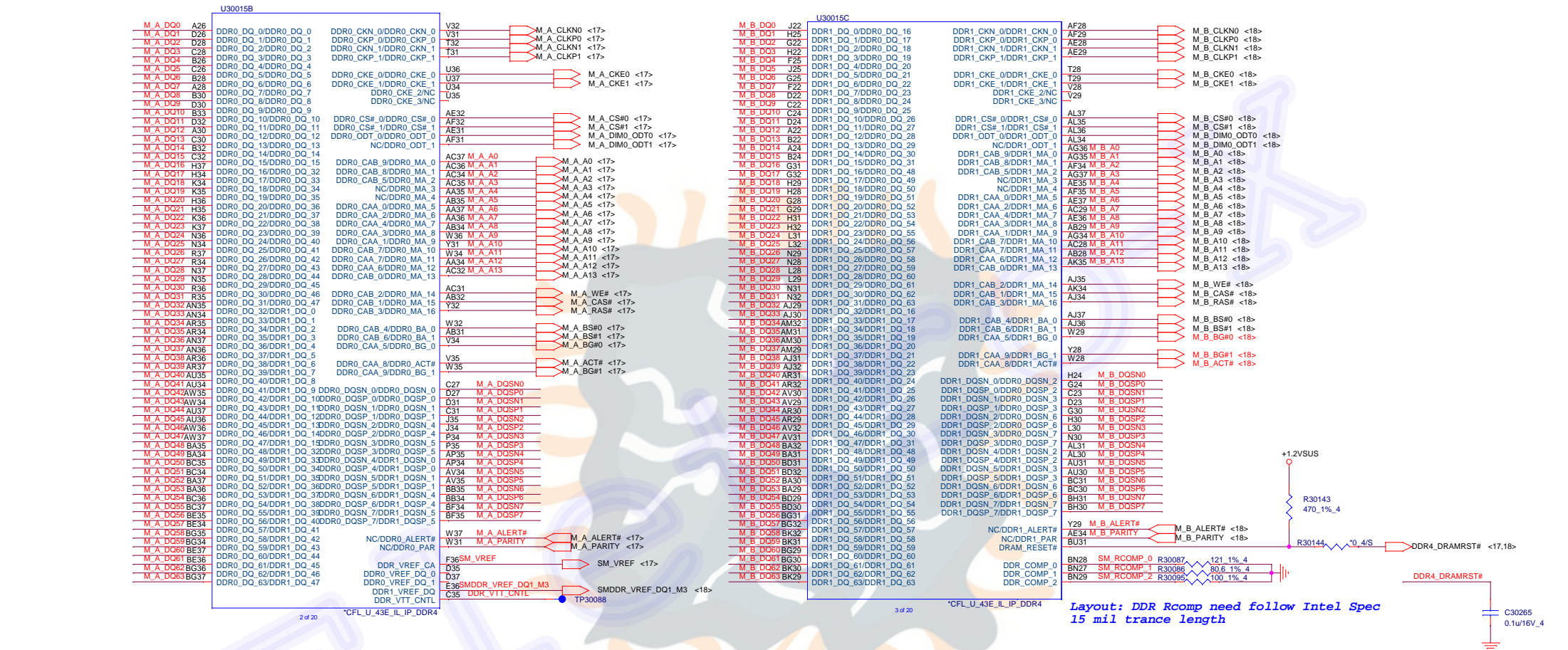
CFL\_U\_43E\_IL\_IP\_DDR4

# WHL ULT Processor (DDR4)

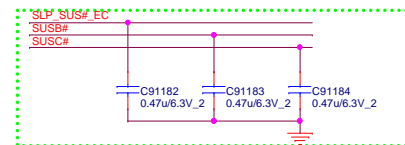
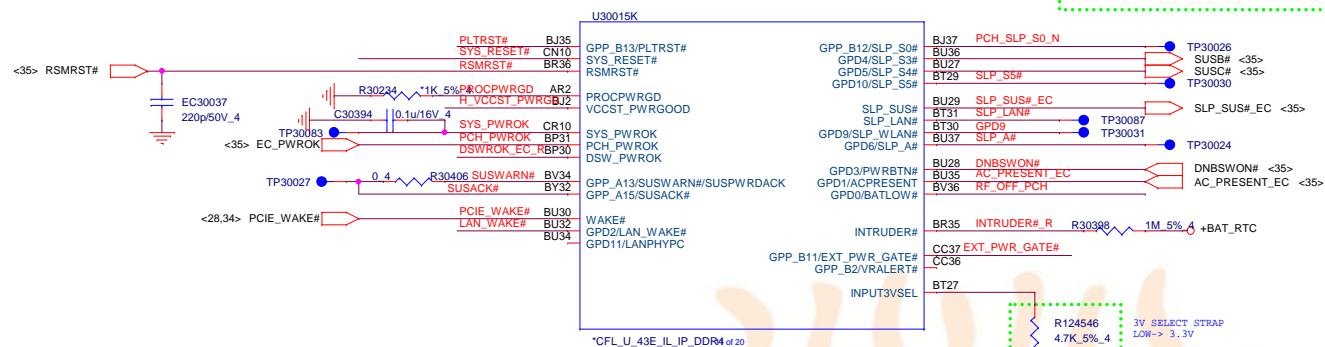
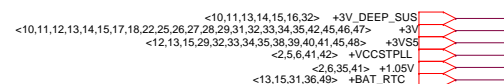
03

## WHL ULT Processor (MEM-A)

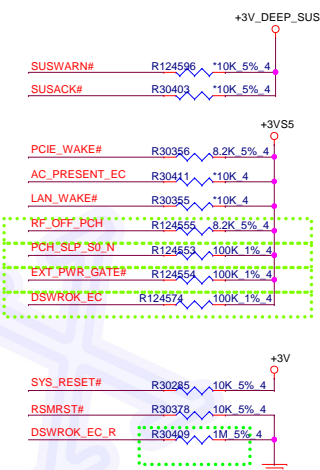
## WHL ULT Processor (MEM-B)



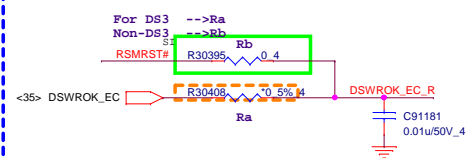




## PCH Pull-high/low(CLG)

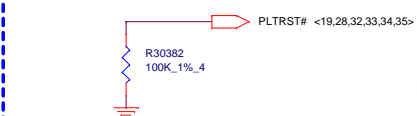


## For DS3 Sequence

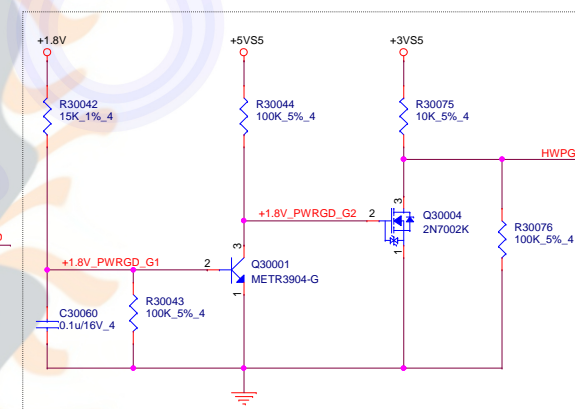
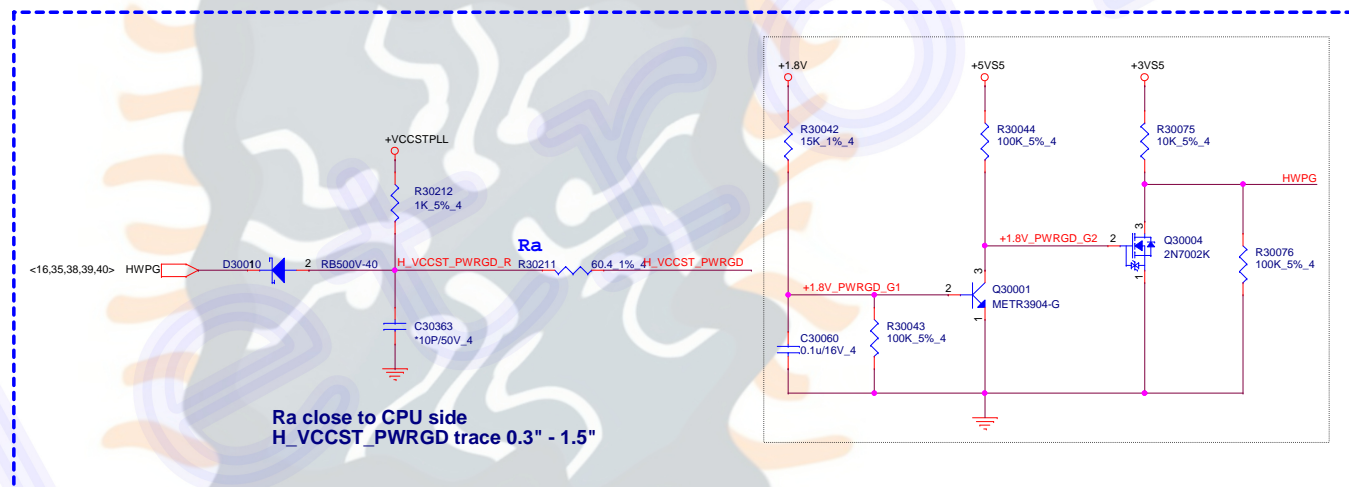
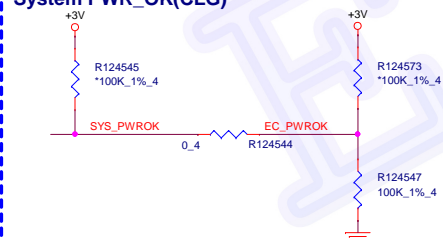


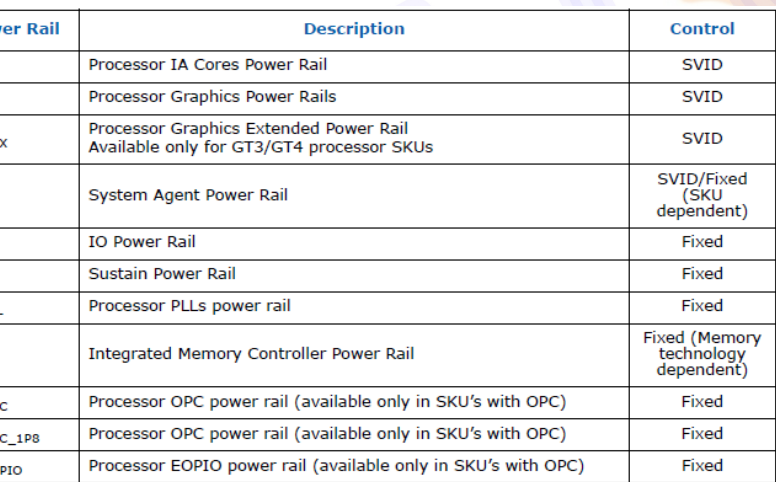
## PLTRST#(CLG)




Check Rise/Fall time less than 100ns

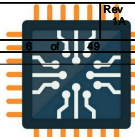
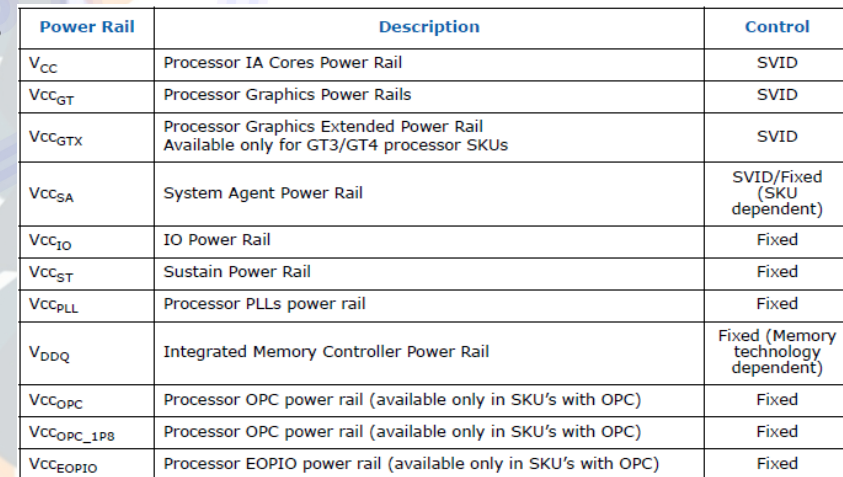


## System PWR\_OK(CLG)



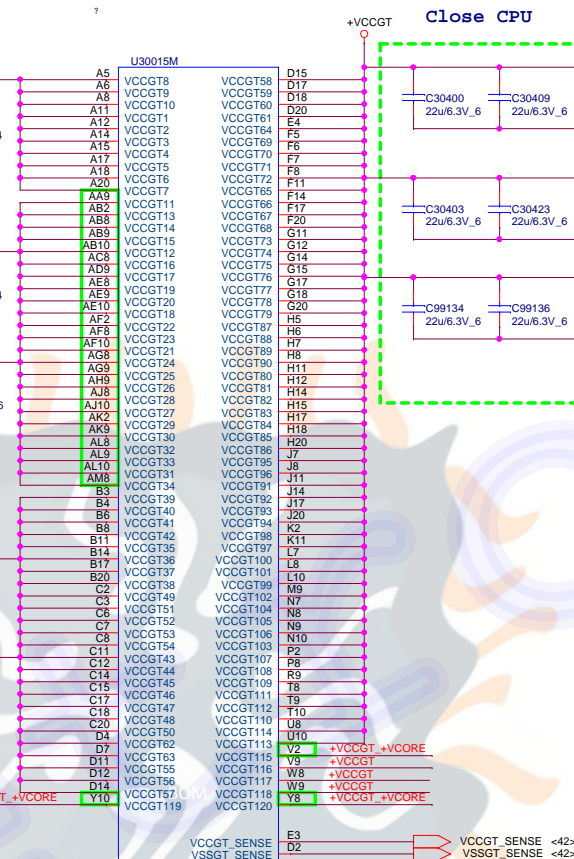
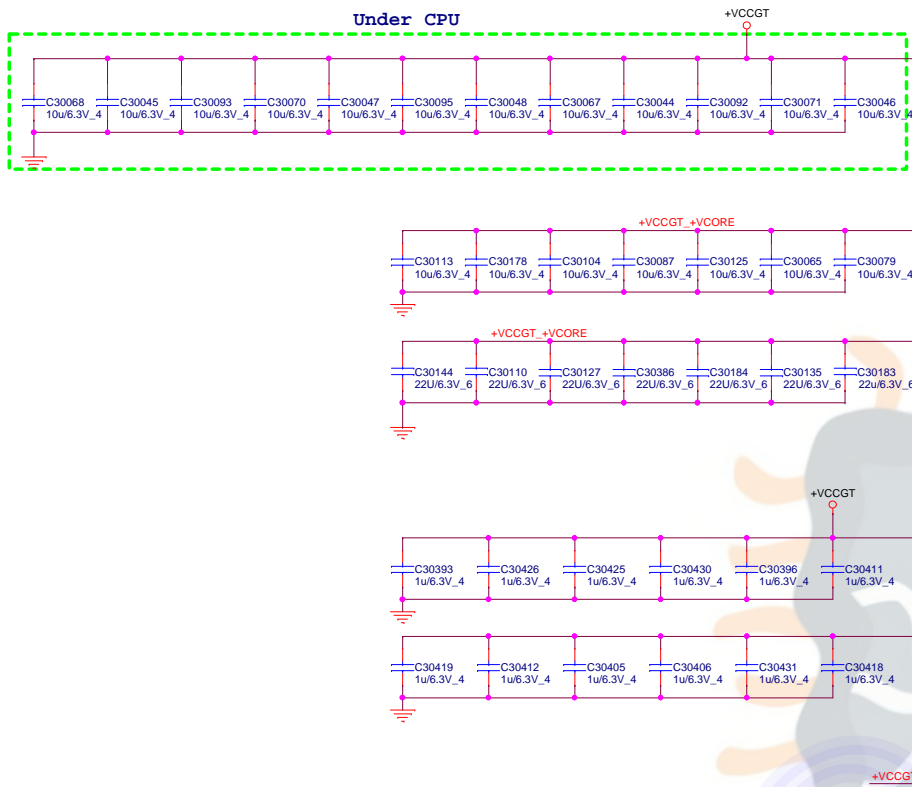


	PROJECT : G7BD		
	Quanta Computer Inc.		
	Size Custom	Document Number <b>KBL-U 4/15 (POWER-1)</b>	
Date: Wednesday, December 26, 2018		Sheet	



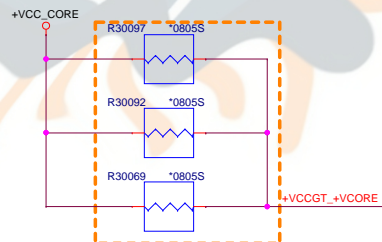
+VCCGT <42,44>  
+VCC\_CORE <45,42,43>  
+1.2VSUS <3,6,17,18,39,41>

## Under CPU

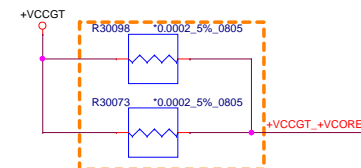


Power Rail	Description	Control
V <sub>CC</sub>	Processor IA Cores Power Rail	SVID
V <sub>CCGT</sub>	Processor Graphics Power Rails	SVID
V <sub>CCGTx</sub>	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V <sub>CCSA</sub>	System Agent Power Rail	SVID/Fixed (SKU dependent)
V <sub>CCIO</sub>	IO Power Rail	Fixed
V <sub>CCST</sub>	Sustain Power Rail	Fixed
V <sub>CCPLL</sub>	Processor PLLs power rail	Fixed
V <sub>DDQ</sub>	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V <sub>CCOPC</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCOPC_1P8</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCEOPIO</sub>	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed


\*CF\_L0:08E\_IL\_IP\_DDR4

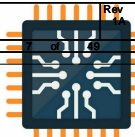


For WHL U42 ES2 上件/0122



For WHL U42 ES1 上件/0122

	PROJECT : G7BD Quanta Computer Inc.	
	Size Custom	Document Number KBL-U 6/15 (POWER-3)
	Date: Wednesday, December 26, 2018   Sheet 1 of 1	





U30015T		
N6	VSS_290	CF23
B37	VSS_291	V4
CB3	VSS_292	BE30
P10	VSS_293	CF28
B5	VSS_294	W10
CB33	VSS_295	BE31
P3	VSS_296	CF3
B7	VSS_297	W27
CB4	VSS_298	CF4
P33	VSS_299	W30
B9	VSS_300	BF3
CB7	VSS_301	CG33
P36	VSS_302	BF33
BA10	VSS_303	CG7
CC11	VSS_304	BF36
P4	VSS_305	Y26
BA28	VSS_306	Y26
P7	VSS_307	BF4
BA3	VSS_308	CH31
CC20	VSS_309	Y27
R27	VSS_310	BG25
BB3	VSS_311	Y30
CC25	VSS_312	BG28
R28	VSS_313	CJ11
BB33	VSS_314	Y33
CC28	VSS_315	CJ14
R29	VSS_316	Y35
BB36	VSS_317	BH28
CC31	VSS_318	CJ19
R30	VSS_319	Y7
BB4	VSS_320	BH29
CC7	VSS_321	CJ23
R31	VSS_322	BH32
BC25	VSS_323	CJ28
CD11	VSS_324	BH33
T27	VSS_325	CJ33
CD12	VSS_326	BH35
T30	VSS_327	CJ35
BC29	VSS_328	BP19
CD14	VSS_329	BR16
T33	VSS_330	BY18
BC32	VSS_331	BY19
CD24	VSS_332	CC16
T36	VSS_333	BU16
CD25	VSS_334	CC14
I7	VSS_335	BR22
BC8	VSS_336	BU20
CE33	VSS_337	CD20
BD28	VSS_338	BT14
CE35	VSS_339	BP12
U7	VSS_340	CB24
BD33	VSS_341	CC24
CE36	VSS_342	J5
V26	VSS_343	U24
BD35	VSS_344	BD7
CE7	VSS_345	AR4
V27	VSS_346	AU4
BD36	VSS_347	AW4
CF11	VSS_348	BA6
BE10	VSS_349	BC4
CF14	VSS_350	BE4
V30	VSS_351	BE8
BE28	VSS_352	BA4
CF19	VSS_353	BD4
V33	VSS_354	BG4
BE29	VSS_355	CJ2
CF2	VSS_356	CJ3
V36	VSS_357	AM5
BE3	VSS_358	CM4
	VSS_359	AC5
	VSS_360	AG5
	VSS_361	CR6
	VSS_362	CR6

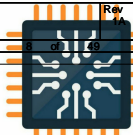
\*CFL\_U\_43E\_IL\_IP\_DDR4

U30015R		
CR34	VSS_1	BL7
BT5	VSS_2	AE25
BY5	VSS_3	BM33
CP35	VSS_4	CM5
CM37	VSS_5	AE27
CH37	VSS_6	BM35
AW1	VSS_7	CM9
CM1	VSS_8	AE30
BD6	VSS_9	BM36
AY4	VSS_10	AE7
B34	VSS_11	BM9
E35	VSS_12	AE27
A4	VSS_13	CM17
AE24	VSS_14	BN30
AE26	VSS_15	CM21
AF25	VSS_16	AF3
AG24	VSS_17	BN7
AG26	VSS_18	CM25
AH24	VSS_19	AF30
AH25	VSS_20	CM29
B2	VSS_21	AF33
B36	VSS_22	BP15
C36	VSS_23	AF36
C37	VSS_24	AF4
CN1	VSS_25	CM5
CN2	VSS_26	CM9
CM37	VSS_27	BP25
CP2	VSS_28	CM9
D1	VSS_29	AG10
A32	VSS_30	CP1
F33	VSS_31	BP3
A3	VSS_32	BP32
BJ7	VSS_33	CP11
CJ38	VSS_34	AE27
A36	VSS_35	BP33
BK10	VSS_36	CP13
CJ4	VSS_37	AH28
AB27	VSS_38	BP4
BK2	VSS_39	CP15
CK1	VSS_40	AH29
AB3	VSS_41	BP7
BK28	VSS_42	CP19
AB30	VSS_43	AH30
BK3	VSS_44	CP21
CK4	VSS_45	AH31
AB33	VSS_46	BR19
BK33	VSS_47	CP27
CK7	VSS_48	AH33
AB36	VSS_49	BR25
BK4	VSS_50	AH35
CL2	VSS_51	CP37
AB4	VSS_52	AJ25
BK7	VSS_53	BT15
CM13	VSS_54	AL28
AB7	VSS_55	BT16
BL25	VSS_56	CP9
CM17	VSS_57	AJ7
AG10	VSS_58	CR2
BL28	VSS_59	AK3
CM21	VSS_60	CR36
AC27	VSS_61	AK33
BL29	VSS_62	D21
CM25	VSS_63	AK36
AC30	VSS_64	BT25
BL30	VSS_65	AK4
CM29	VSS_66	BT28
BL31	VSS_67	AL28
CM31	VSS_68	BT33
AD33	VSS_69	D5
BL32	VSS_70	AL29
CM33	VSS_71	
AD35	VSS_72	

\*CFL\_U\_43E\_IL\_IP\_DDR4

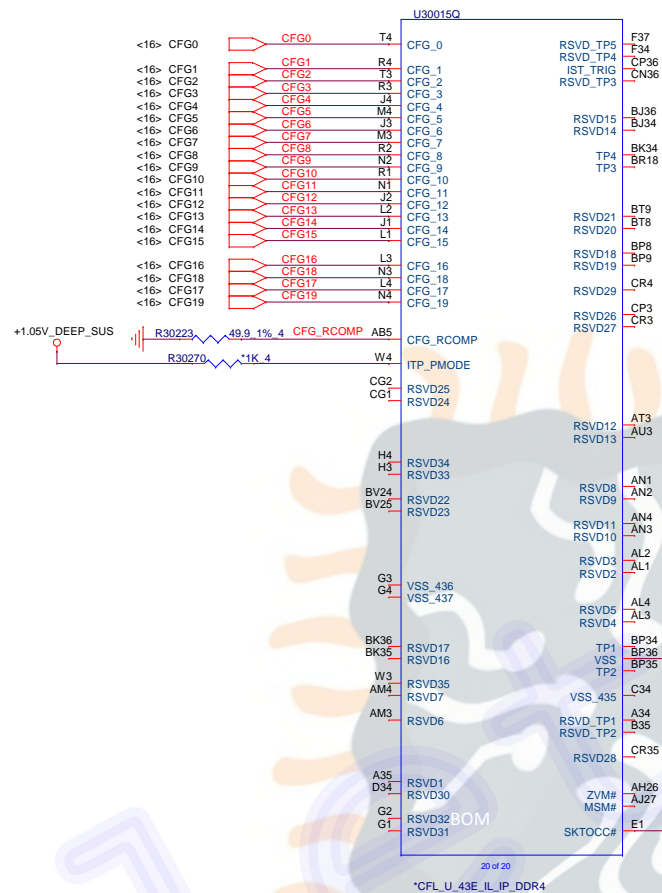
U30015S		
BT35	VSS_145	BY25
D6	VSS_146	J18
AL32	VSS_147	AU32
BT36	VSS_148	BY28
D8	VSS_149	J21
AL7	VSS_150	AV25
D9	VSS_151	BY33
AM10	VSS_152	J24
BU11	VSS_153	AV28
E23	VSS_154	BY35
AM28	VSS_155	J33
E27	VSS_156	AV3
AM33	VSS_157	BY36
BU23	VSS_158	J36
E29	VSS_159	AV33
AM35	VSS_160	J6
BU24	VSS_161	AV36
E31	VSS_162	C1
BU25	VSS_163	K21
E33	VSS_164	AV4
AN25	VSS_165	C21
BU7	VSS_166	K22
E9	VSS_167	AV6
AN28	VSS_168	C25
BU11	VSS_169	K24
F12	VSS_170	AV8
AM29	VSS_171	C29
F15	VSS_172	K25
AN30	VSS_173	AW28
F18	VSS_174	C33
AN31	VSS_175	K27
BU3	VSS_176	AW29
F2	VSS_177	C4
AN7	VSS_178	K28
BU31	VSS_179	AW3
F21	VSS_180	C9
AN8	VSS_181	K29
BU33	VSS_182	AW30
F24	VSS_183	CA11
BU4	VSS_184	K3
F3	VSS_185	AW31
AP3	VSS_186	CA15
BW11	VSS_187	K30
F4	VSS_188	AY33
AP33	VSS_189	CA22
BW15	VSS_190	K31
G21	VSS_191	AY35
AP36	VSS_192	K32
G27	VSS_193	B12
AP4	VSS_194	K4
G33	VSS_195	B15
AR28	VSS_196	CA25
G35	VSS_197	K9
G36	VSS_198	B18
AT33	VSS_199	CB11
BW24	VSS_200	L27
G9	VSS_201	B21
AT35	VSS_202	B23
H21	VSS_203	L35
AT36	VSS_204	B25
BW7	VSS_205	CB18
H27	VSS_206	L36
AT4	VSS_207	B27
BY11	VSS_208	CB19
AU10	VSS_209	L6
BY15	VSS_210	B29
H9	VSS_211	CB2
AT28	VSS_212	N25
BY22	VSS_213	B31
J12	VSS_214	CB20
AU29	VSS_215	N27
J15	VSS_216	CB25
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	VSS_286	
	VSS_287	
	VSS_288	
	VSS_289	

\*CFL\_U\_43E\_IL\_IP\_DDR4





+1.05V\_DEEP\_SUS <15,33,40,41>



**Processor Strapping** The CFG signals have a default value of '1' if not terminated on the board.

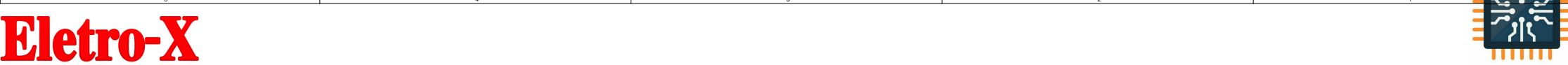
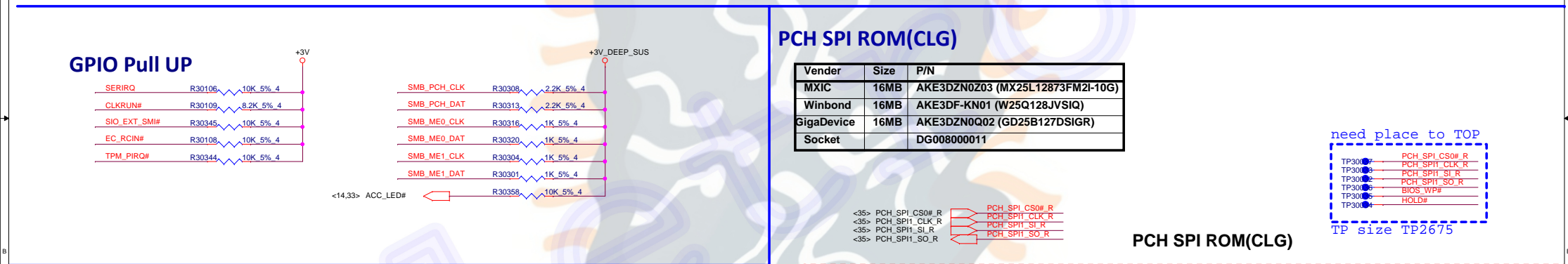
	1	0	Circuit
CFG3 (Physical Debug Enable) DFX_Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	

**PROJECT : G7BD**  
**Quanta Computer Inc.**

Size  
Custom

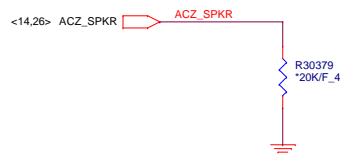
Document Number  
**KBL-U 8/15 (RSV)**

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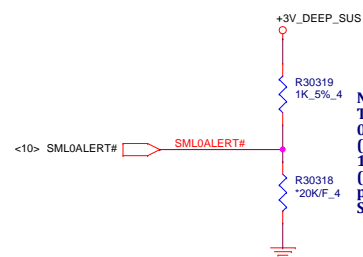


# Functional Strap Definitions

**DESIGN NOTE:**  
WEAK PULL UP RESISTOR PRESENT ON THIS NET



**TOP SWAP OVERRIDE**  
HIGH - TOP SWAP ENABLE  
LOW-DISABLED  
HIGH: LPC SELECTED FOR SYSTEM FLASH  
WEAK INTERNAL PD



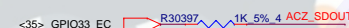
**No Boot:**  
The signal has a weak internal pull-down.  
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).  
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



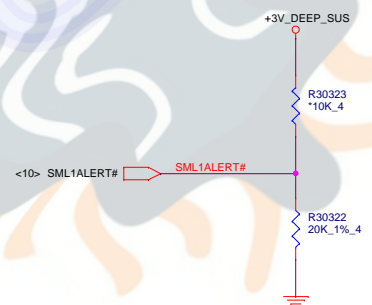
**No Boot:**  
The signal has a weak internal pull-down.  
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.  
Bit 10      Boot BIOS Destination  
0            SPI  
1            LPC




**No Boot:**  
The signal has a weak internal pull-down.  
0 = Enable security measures defined in the Flash Descriptor.  
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



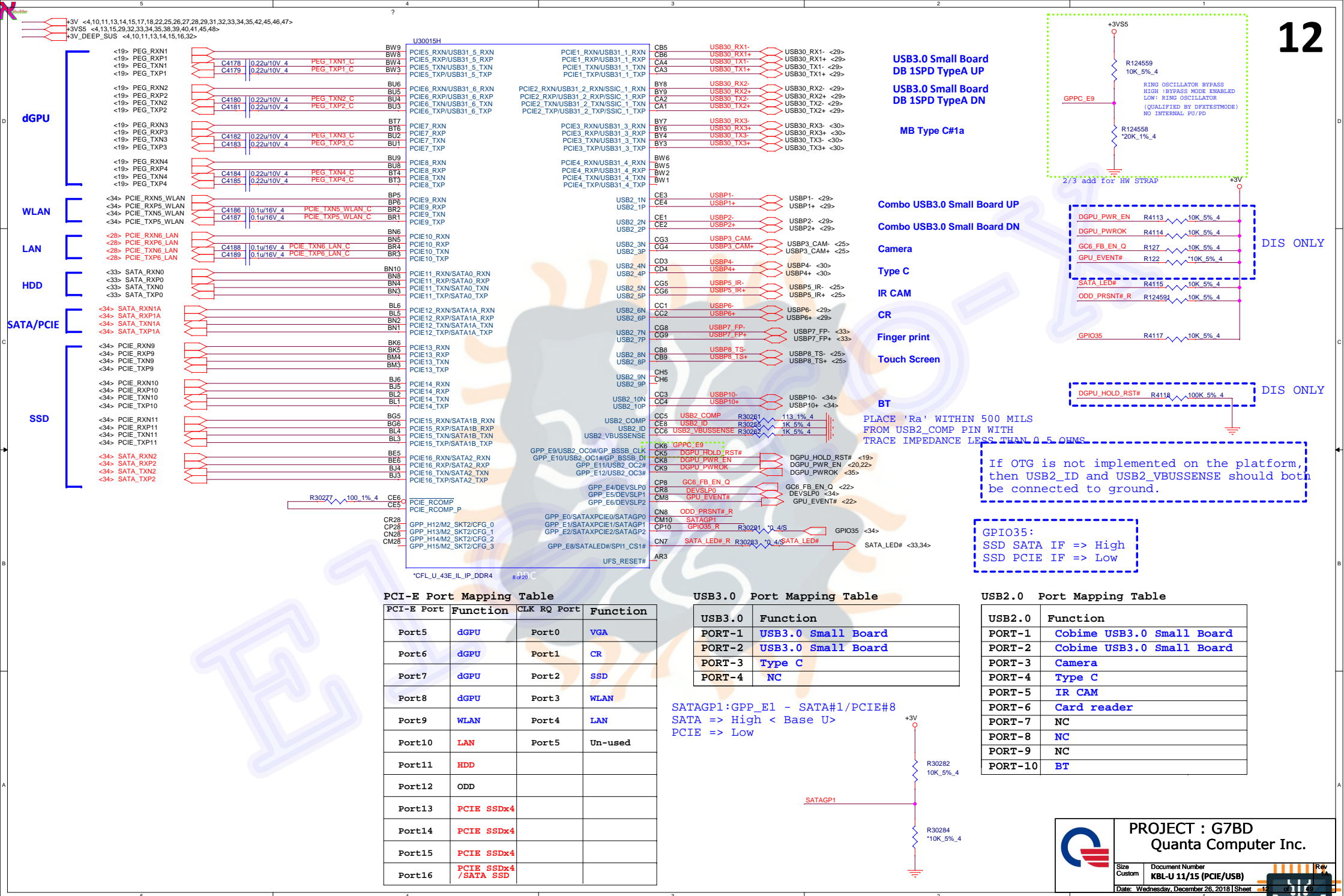
**No Boot:**  
The signal has a weak internal pull-down.  
0 = Disable No Reboot mode.  
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

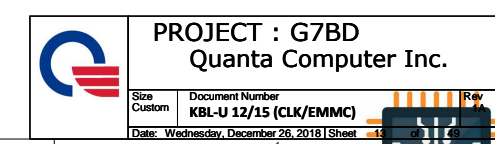


**No Boot:**  
The signal has a weak internal pull-down.  
0 = LPC is selected for EC.  
1 = eSPI is selected for EC.

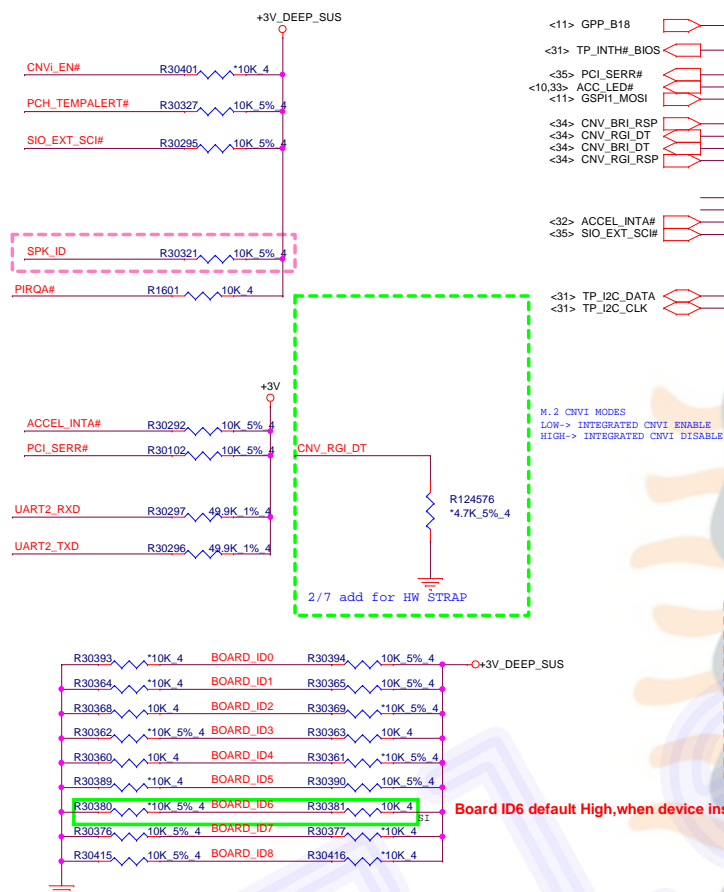
		PROJECT : G7BD	
		Quanta Computer Inc.	
Size Custom	Document Number KBL-U 10/15(HDA)	Rev 1.0	
Date: Wednesday, December 26, 2018   Sheet 11		of 10	







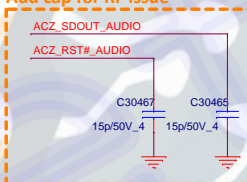
## WHLake (GPIO)



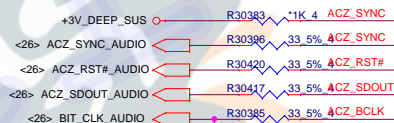
Board ID6 default High, when device insert will become low

WHL	BOARD_ID[8:7]	Board ID 6	Board ID 5	Board ID 4	BOARD_ID[3:1]	BOARD_ID0
Model	ID8 ID7	ID6	ID5	ID4	ID3 ID2 ID1	ID0
Definition	Reserve (Default = 00)	0: Finger Print 1: Non-Finger Print	0: AMD 1: Nvidia GPU setting	0: 2G VRAM 1: 4G VRAM	100: 14" (WHL) 000: 14" 101: 15" 1SPD (WHL) 001: 15 1SPD 110: 2SPD (WHL) 010: MAX-Q 111: 13" (WHL) 011: 2SPD	0: UMA 1: DIS

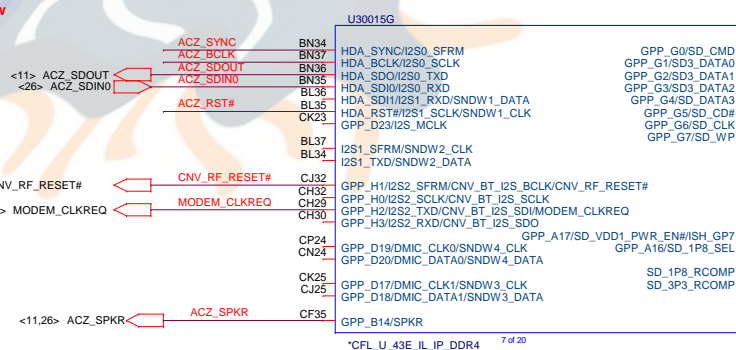
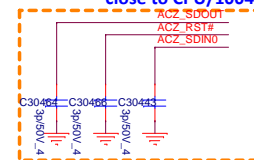
Add cap for RF issue



## HDA Bus (CLG)



close to CPU/1004

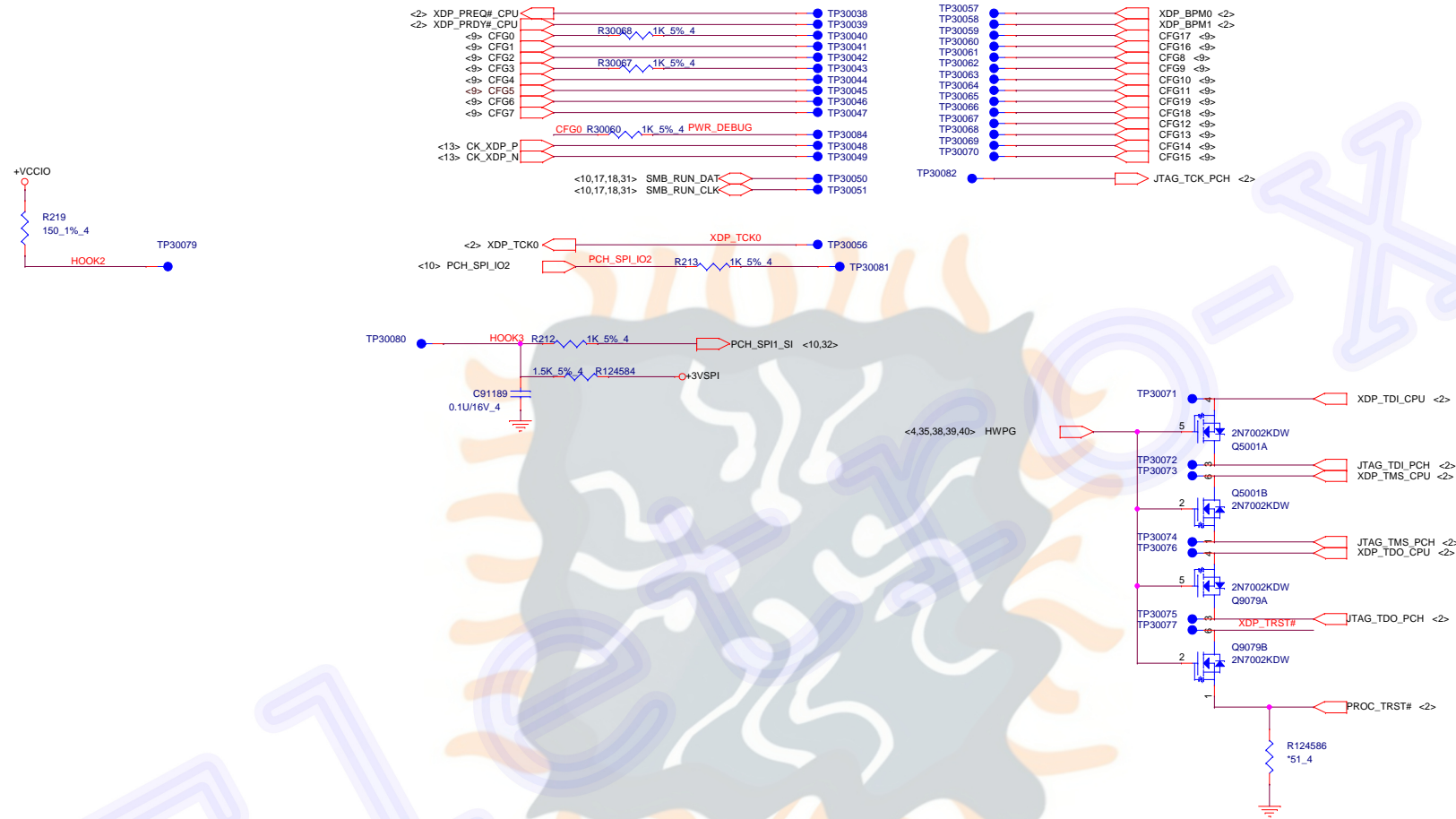


**PROJECT : G7BD**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>KBL-U 13/15 (GPIO)</b>
Date: Wednesday, December 26, 2018   Sheet 14 of 19	

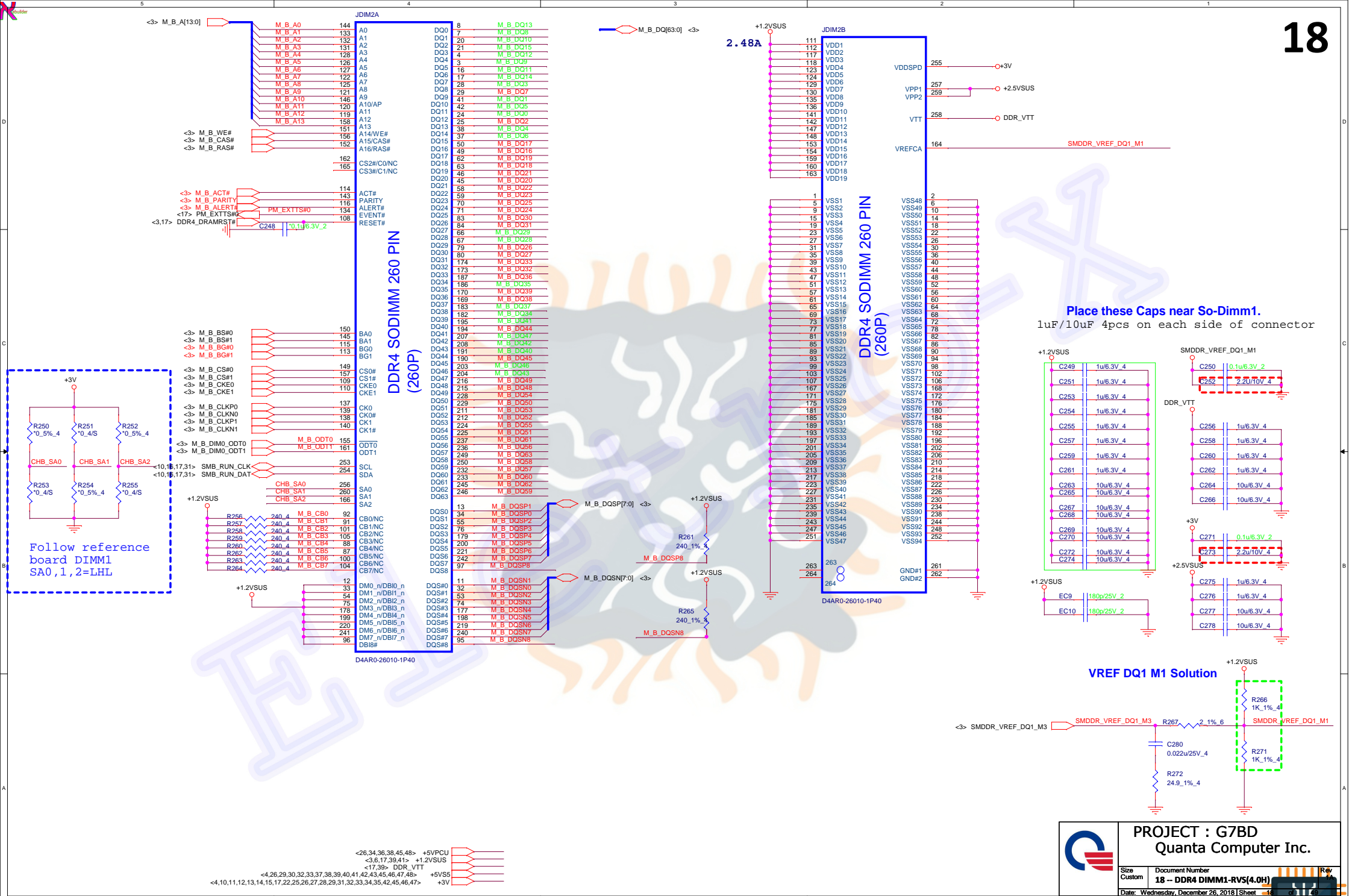




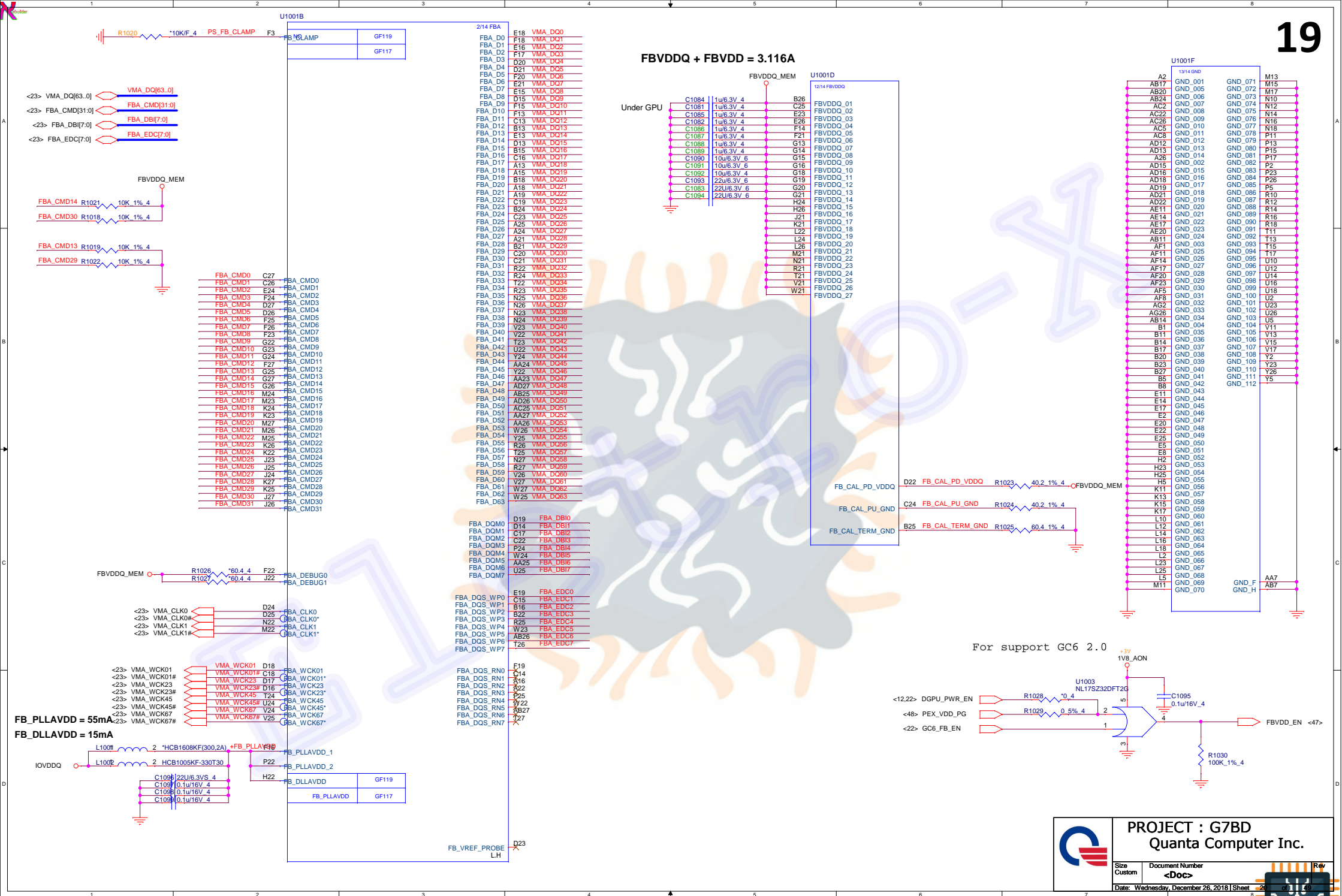




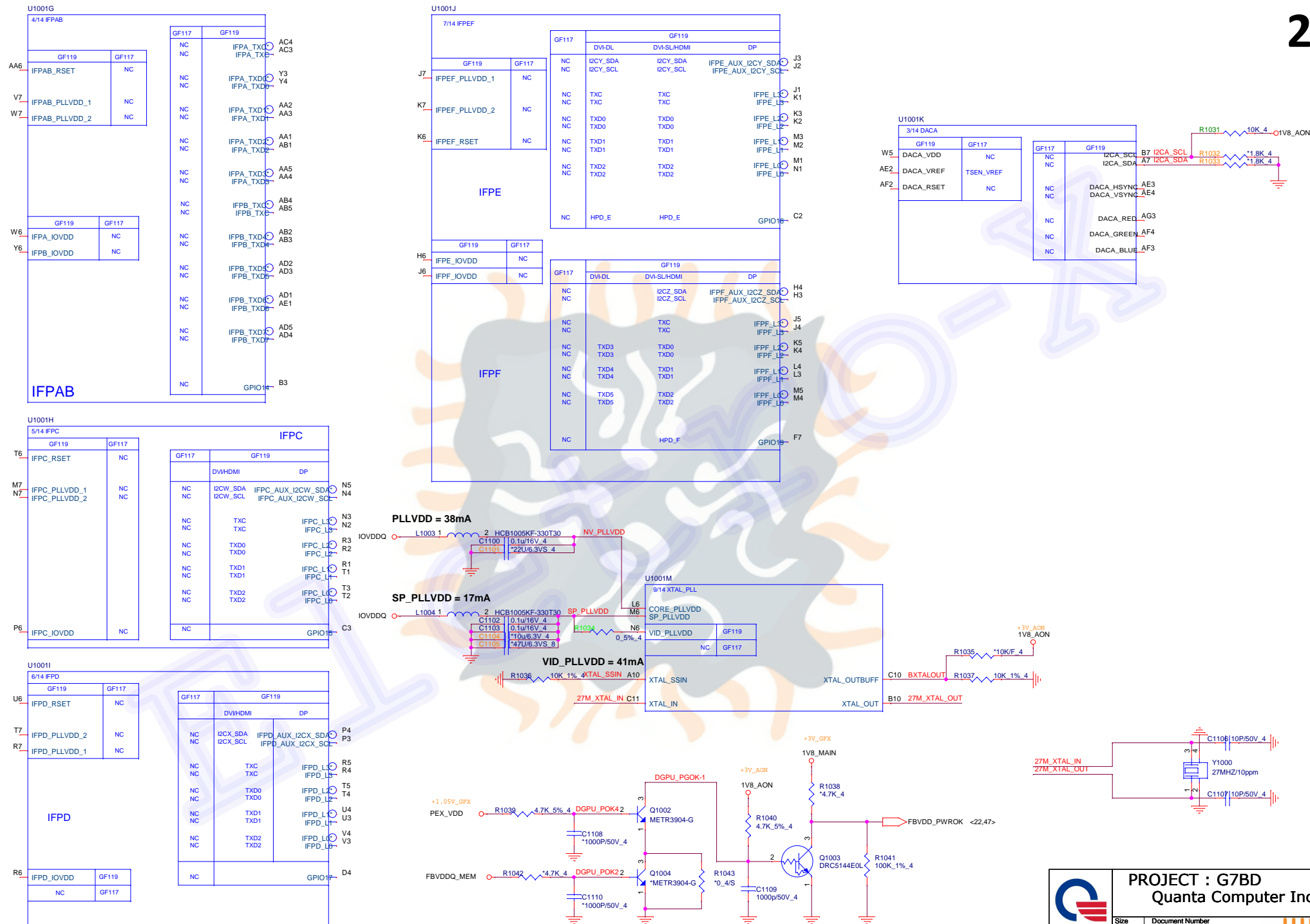








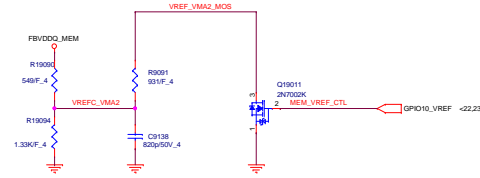
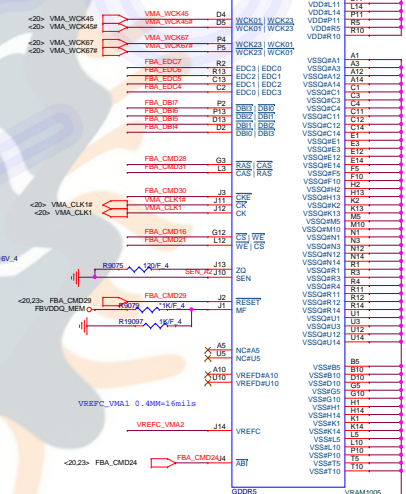
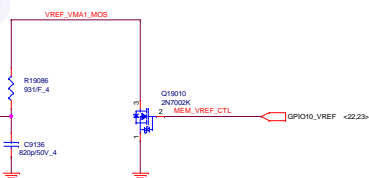






Channel A  
<32-63>

MF=0 Non-mirrored



GDDR5 256 x 32	Hynix H5G8C8H24MJR-R0C	AKG5QGUTW04	AKG5QGUTW03
	Micron MT51J256M32HF-70:A	AKG5QGUTL07	AKG5QGUTL06
	Samsung K4G80325FB-HC28	AKG5QGDT509	AKG5QGDT508



<b>N16S strap setting</b>	
ROM_SI	• VRAM Configuration follow VRAM table
ROM_S0	• Stuff 4.98K Pull Up <b>CS14892P25</b>
ROM_S256	• Stuff 4.98K Pull Down <b>CS14892P25</b>
STRAP0	• Stuff 49.9K Pull Up <b>CS14892P10</b>
STRAP1	• NC
STRAP2	• NC
STRAP3	• NC
STRAP4	• NC
STRAP5	• NC
<b>N17S strap setting</b>	
ROM_SI	• Stuff 100K Pull Up <b>CS41002P20</b>
ROM_S0	• Stuff 100K Pull Up <b>CS41002P20</b>
ROM_S256	• Stuff 100K Pull Up and 100K Pull Down <b>CS41002P20</b>
STRAP0	• VRAM Configuration follow VRAM table
STRAP1	• VRAM Configuration follow VRAM table
STRAP2	• VRAM Configuration follow VRAM table
STRAP3	• Stuff 100K Pull Down <b>CS41002P20</b>
STRAP4	• Stuff 100K Pull Down <b>CS41002P20</b>
STRAP5	• Stuff 100K Pull Down <b>CS41002P20</b>

	STRAP2	STRAP1	STRAP0	
Samsung	L	L	L	0x0000
Micron	H	L	L	0x0004
Hynix	H	L	H	0x0005

STRAP[2:0] VRAM Table for N17S-G1 GDDR5 Recommended Memories

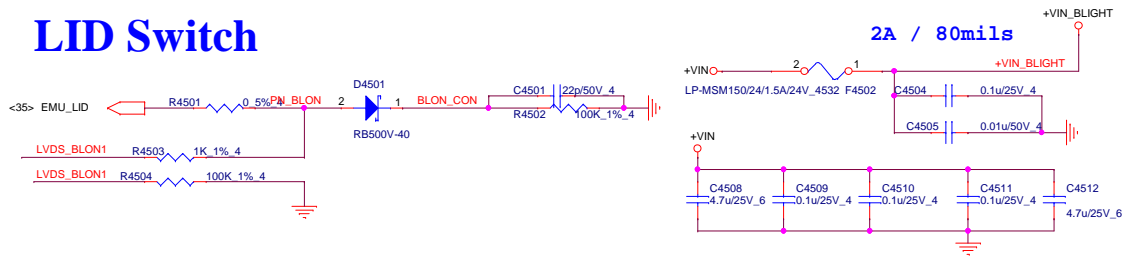
BANK# [2:0]	DESCRIPTION	Vendor	Vendor P/N	TOP P/N	QB P/N
0x0	GDDR5 512Mx16 7 GHz	Samsung B die	K4G80325FB-BC28	<b>AKG5QGDTS09</b>	AKG5QGDTS08
0x4	GDDR5 512Mx16 8 GHz	Micron B die	MT51J256M32HF-80:B	<b>AKG5QGUTL24</b>	AKG5QGUTL25
0x5	GDDR5 512Mx16 8 GHz	Hynix A die	H5GC8H24AJR-R2C	<b>AKG5QGUTW15</b>	AKG5QGUTW16

ROM\_SI VRAM Table for N16S-GTR GDDR5 Recommended Memories

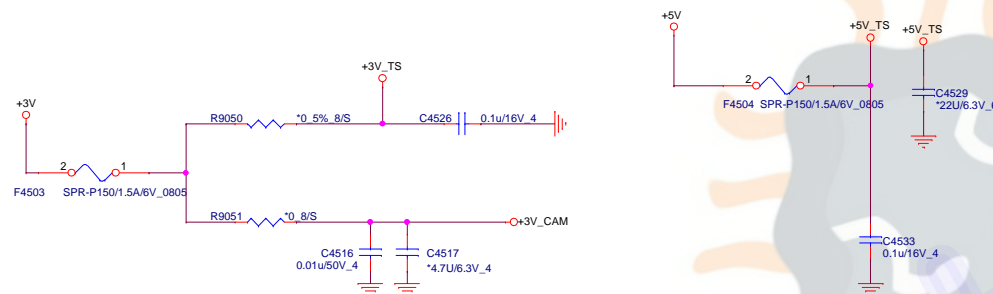
ROM_SI	DESCRIPTION	Vendor	Vendor P/N	TOP P/N	QB P/N
0x0	GDDR5 512Mx16 7 GHz	Samsung B die	K4G80325FB-BC28	<b>AKG5QGDTS09</b>	AKG5QGDTS08
0x8	GDDR5 512Mx16 8 GHz	Micron B die	MT51J256M32HF-80:B	<b>AKG5QGUTL24</b>	AKG5QGUTL25
0x9	GDDR5 512Mx16 8 GHz	Hynix A die	H5GC8H24AJR-R2C	<b>AKG5QGUTW15</b>	AKG5QGUTW16

R1055	SAMSUNG	0000	4.98K	CS24992P25
R1046	HYUNIX	1001	10K	CS11002P25

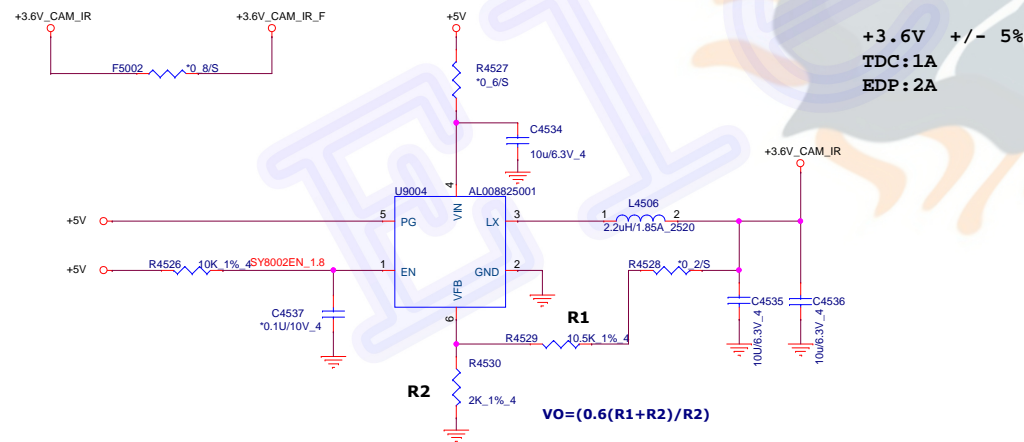
## LID Switch



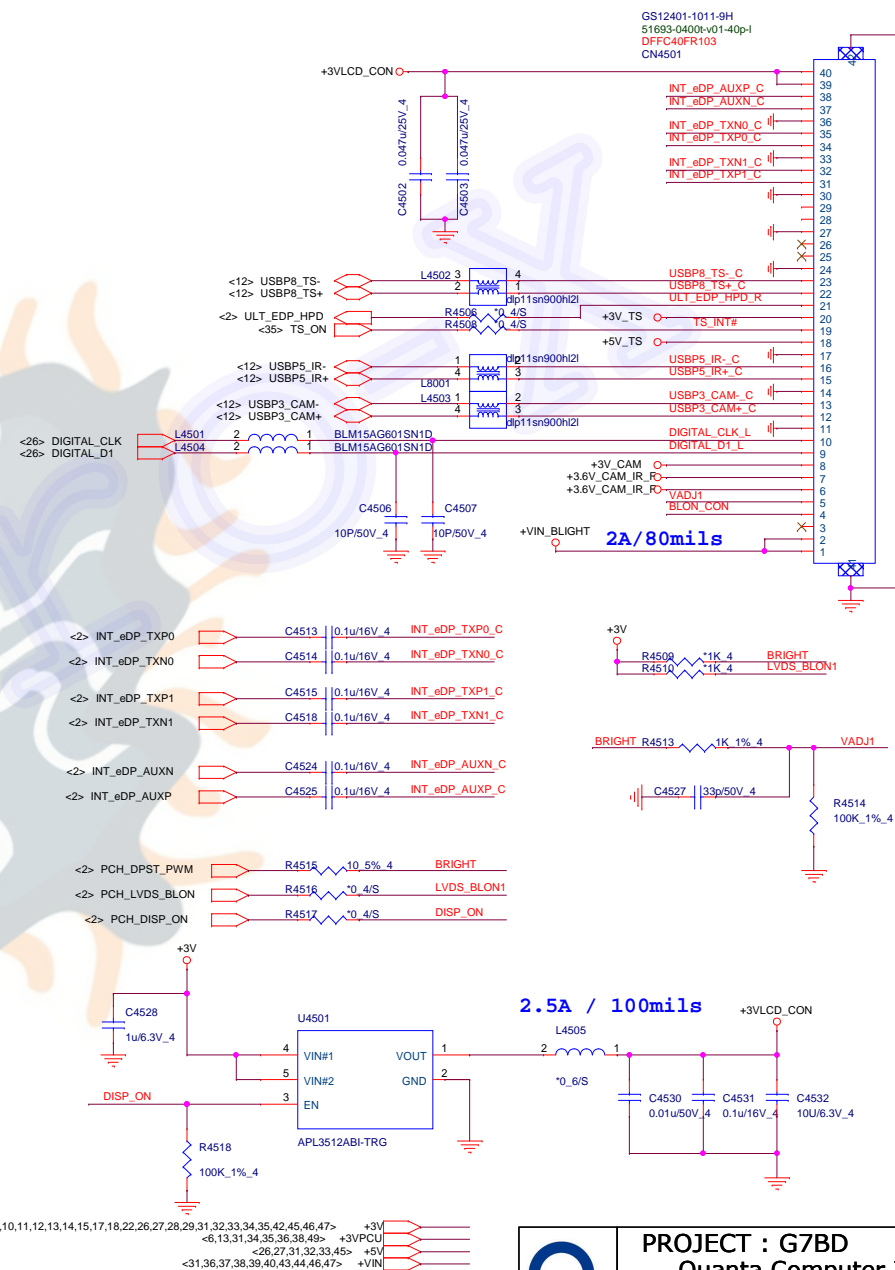
## Touch screen

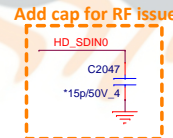
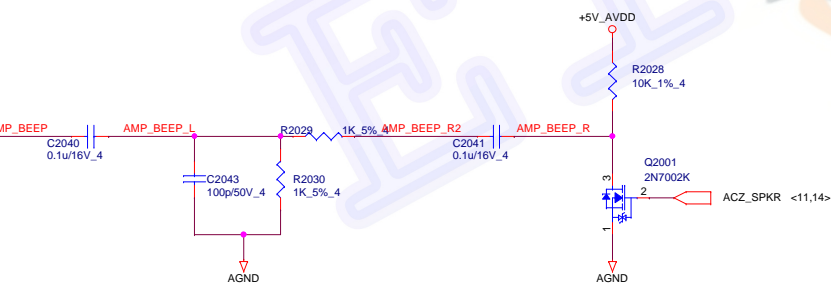
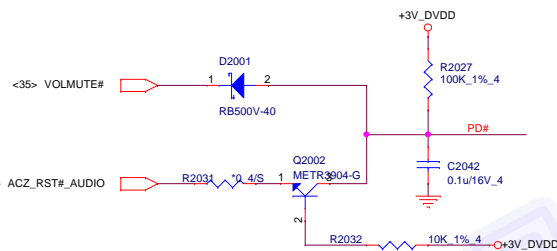
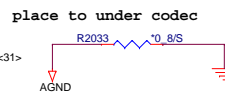
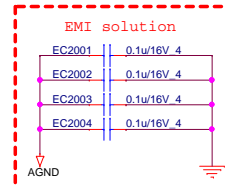
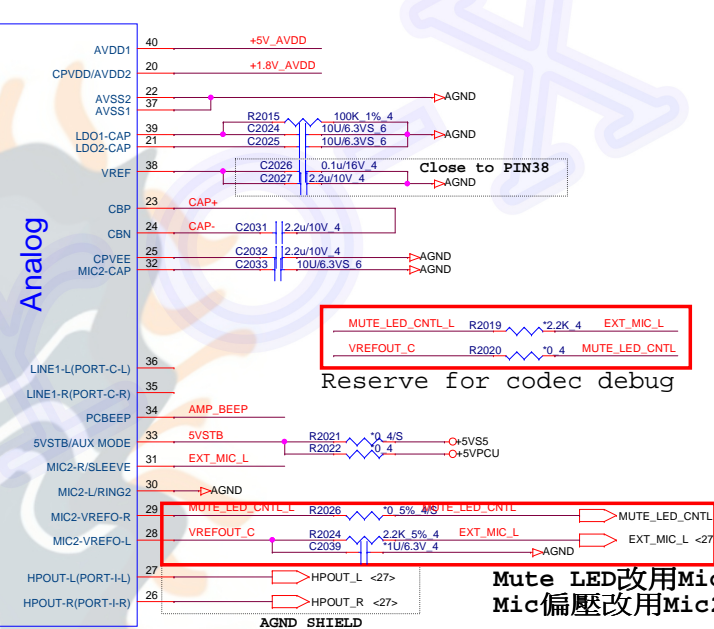
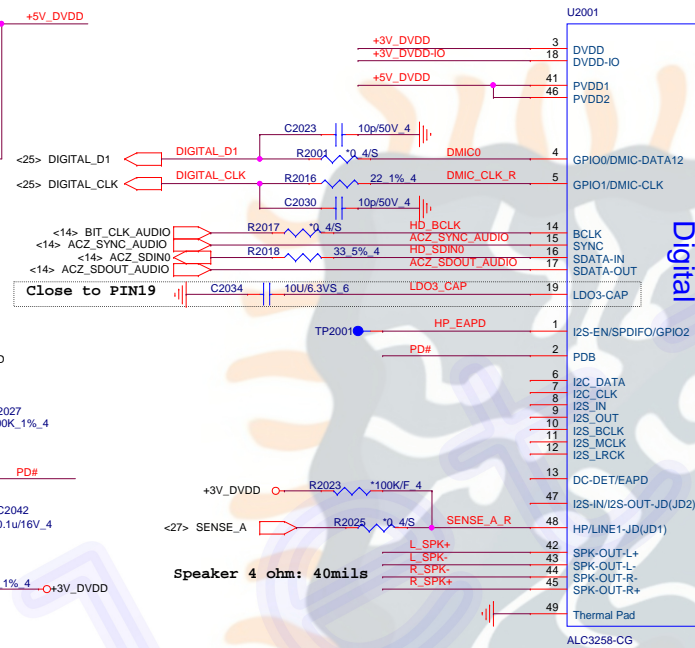
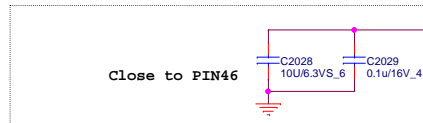
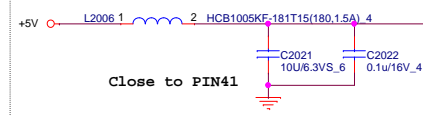
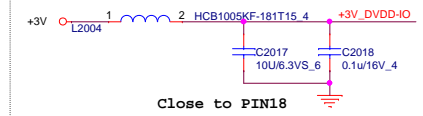
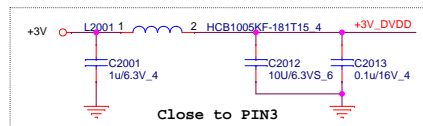


## IR CAM

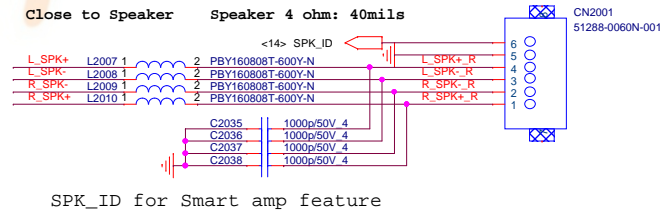


## eDP Conn.





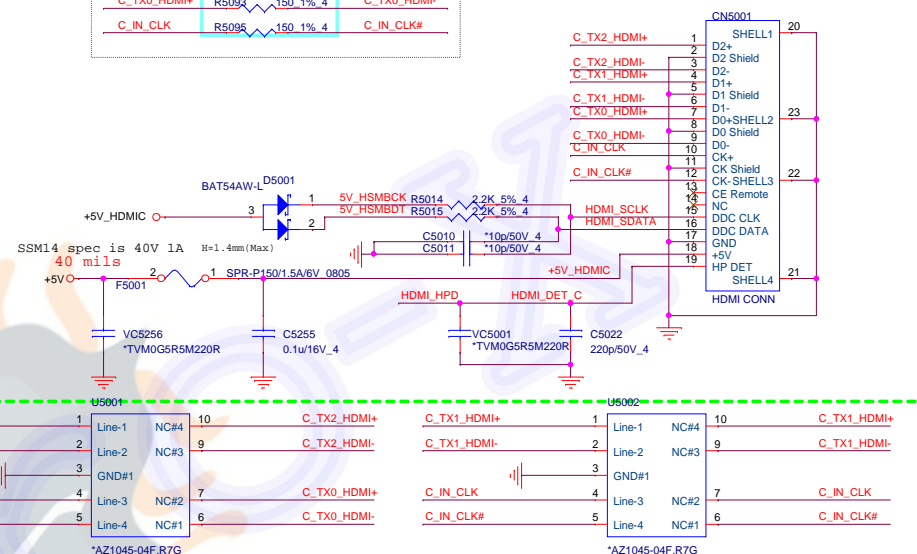
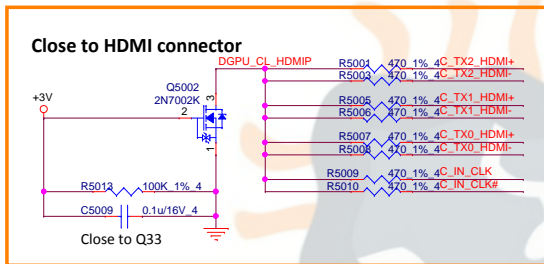
## SPK CONN



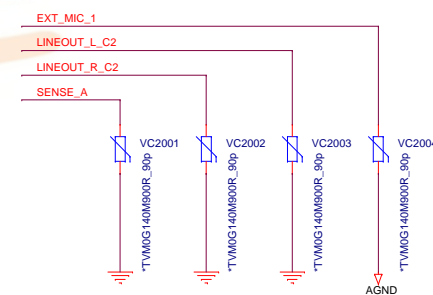
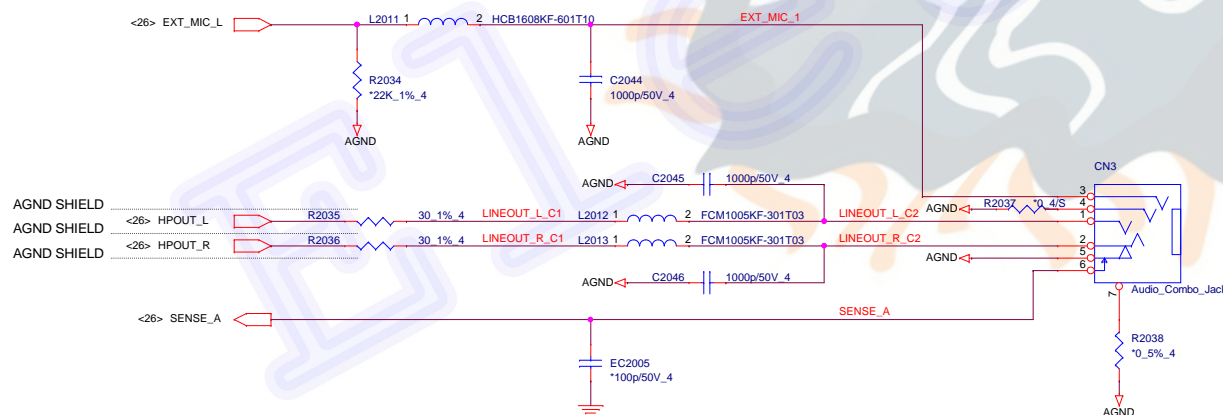
PROJECT : G7BD Quanta Computer Inc.	
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# Eletro-X



## Audio JACK ESD



	<b>PROJECT : G7BD</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number <b>29 – HDM/VAMP HPA0208000000</b>	Rev <b>001</b>
	Date: <b>Wednesday, December 26, 2018</b> Sheet <b>29</b> of <b>40</b>		

\* Place Cc,Cd,Ce,Cf for RTL8107ESH-CG/RTL8111HSH-CG close to each VDD10 pin-- 3, 22, 8 , 30

\* Place Cg,Ch for RTL8107ESH-CG/RTL8111HSH-CG close to each VDD10 pin-- 22(reserved)

Pin configuration diagram for the RTL8111HSH-CG and RTL8107ESH-CG modules. The diagram shows two modules with their respective pin numbers and functions. The RTL8111HSH-CG module has pins 1-8 for MDIO+, MDIO-, MDIO1+, MDIO1-, MDIO2+, MDIO2-, MDIO2, and MDIO2. The RTL8107ESH-CG module has pins 9-16 for MDIO3+, MDIO3-, MDIO3, MDIO3, MDIO3, MDIO3, MDIO3, and MDIO3. The diagram also shows the connection of the modules to the system power and ground pins: +1.05V\_LAN\_O, +1.05V\_LAN\_I, +3V\_LAN, and +3V\_LAN. The RTL8111HSH-CG module is connected to the +1.05V\_LAN\_O and +1.05V\_LAN\_I pins. The RTL8107ESH-CG module is connected to the +3V\_LAN and +3V\_LAN pins. The diagram also shows the connection of the modules to the system power and ground pins: +1.05V\_LAN\_O, +1.05V\_LAN\_I, +3V\_LAN, and +3V\_LAN. The RTL8111HSH-CG module is connected to the +1.05V\_LAN\_O and +1.05V\_LAN\_I pins. The RTL8107ESH-CG module is connected to the +3V\_LAN and +3V\_LAN pins.

For GbE  
\* Place RTL8111HSH-CG AL008111014

For 10/100  
\* Place RTL8107ESH-CG AL008107000

Ub

U3003

MDI2+ 2  
MDI2- 3  
MDI3+ 5  
MDI3- 6  
MDI0+ 8  
MDI0- 9  
MDI1- 11  
MDI1+ 12

MDI2+ 1  
MDI2- 2  
MDI3+ 3  
MDI3- 4  
MDI0+ 5  
MDI0- 6  
MDI1- 7  
MDI1+ 8

TRA\_V\_DAC 1  
TRA\_V\_DAC 4  
TRA\_V\_DAC 7  
TRA\_V\_DAC 10

MCT1 21  
MCT2 18  
MCT3 17  
MCT4 15

LAN\_MCTG0 Ra R3016 75.1% 4  
LAN\_MCTG1 Rb R3017 75.1% 4  
LAN\_MCTG2 Rc R3018 75.1% 4  
LAN\_MCTG3 Rd R3019 75.1% 4

C99148  
0.01uF 50V 4

NS9892407

For GIGA  
BOT:G5T5009 LF,DBOZ06LAN00

FCE:NS892407,DBOLL1LAN00

For 10/100 : Ra,Rb  
For Giga : Ra,Rb,Rc,Rd

C3021  
10p3KV\_1808

For 10/100 : Ra,Rb  
For Giga : Ra,Rb,Rc,Rd

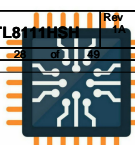
Diagram illustrating the pin connections for the CN3001 component, showing the RJ45\_CONN interface and the DFTJ08FR733 component. The component is labeled (j45-2j)1754-0032111-8p.

Pin connections shown:

- MDI3- 1 (Pin 8)
- MDI3+ 1 (Pin 7)
- MDI1- 1 (Pin 6)
- MDI2- 1 (Pin 5)
- MDI2+ 1 (Pin 4)
- MDI1+ 1 (Pin 3)
- MDI0- 1 (Pin 2)
- MDI0+ 1 (Pin 1)
- RX1- (Pin 8)
- RX1+ (Pin 7)
- RX0- (Pin 6)
- RX0+ (Pin 5)
- TX1- (Pin 4)
- TX1+ (Pin 3)
- RX0+ (Pin 2)
- TX0- (Pin 1)
- TX0+ (Pin 1)
- GND2 (Pin 9)
- GND1 (Pin 10)
- GND3 (Pin 11)
- GND4 (Pin 12)

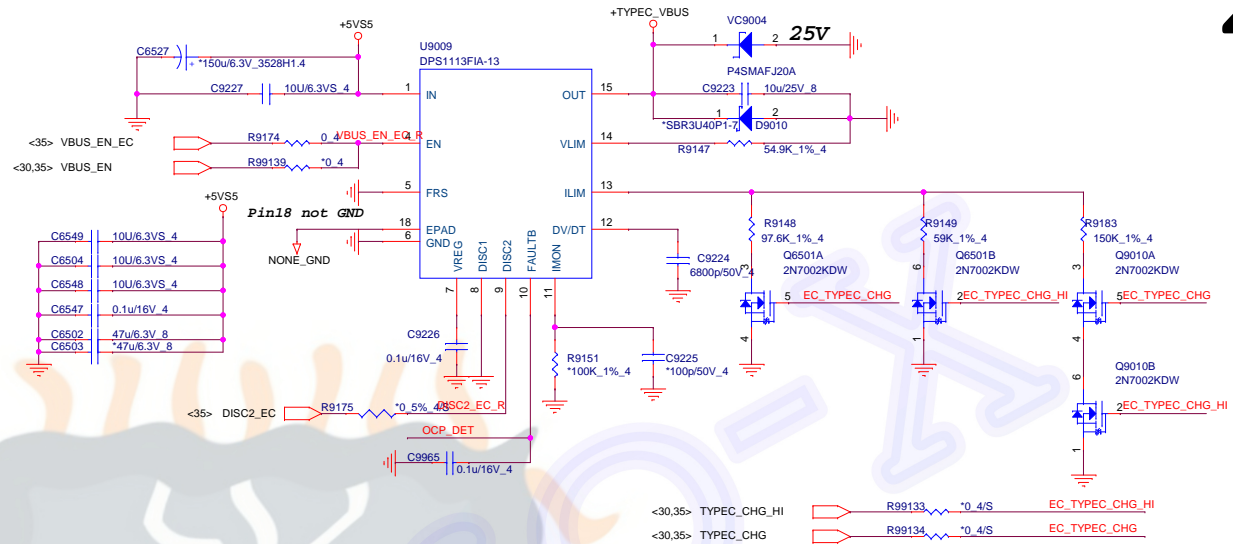
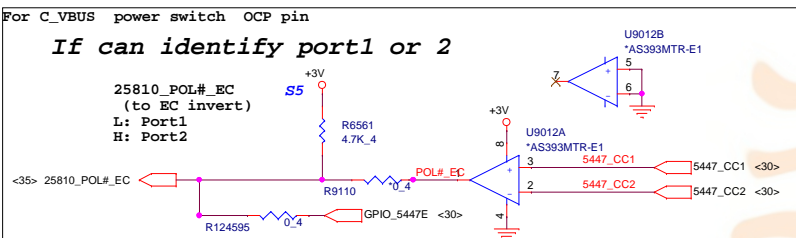
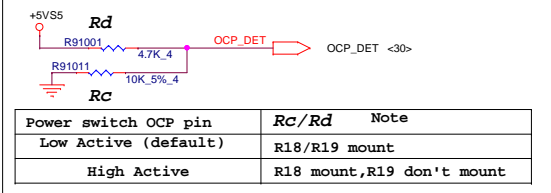
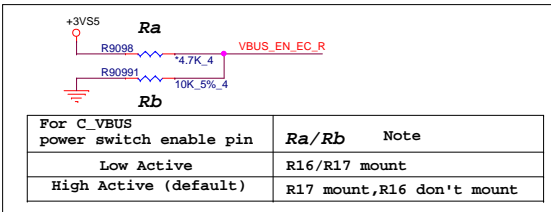
External components connected to the pins:

- R99129 0.5% 6/S (Resistor connected to GND2 and GND1)
- R99128 0.5% 6/S (Resistor connected to GND3 and GND4)

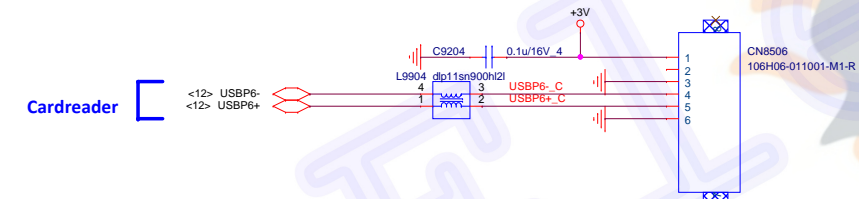


# USB TYPEC POWER SWITCH

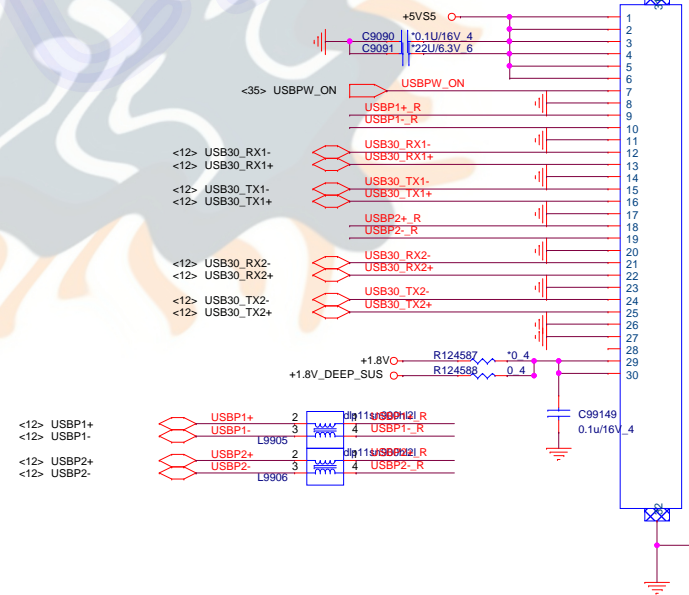
29



## SD Board



## USB Board



CN5502  
DFFC30FR148  
51519-03001-V01-30p-I  
51519-0300T-V01

**PROJECT : G7BD**

**Quanta Computer Inc.**

Size Custom

Document Number **31 -- USB3.0/DB**

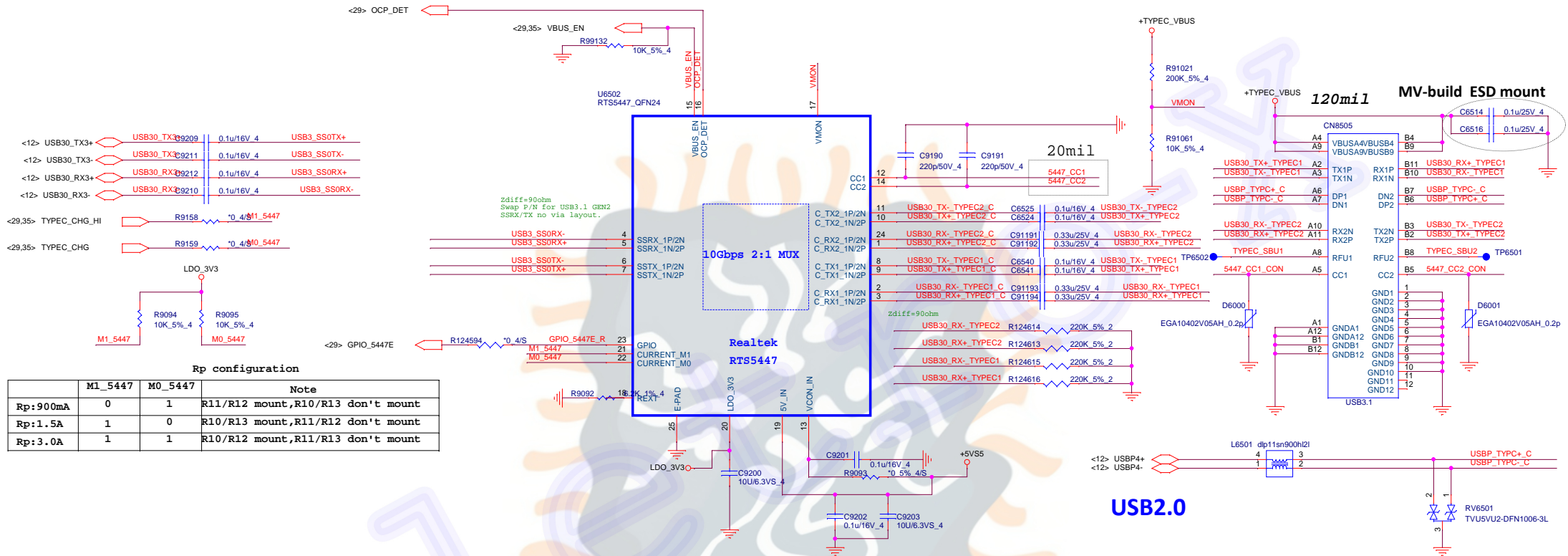
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# TYPE C MUX RTS5447

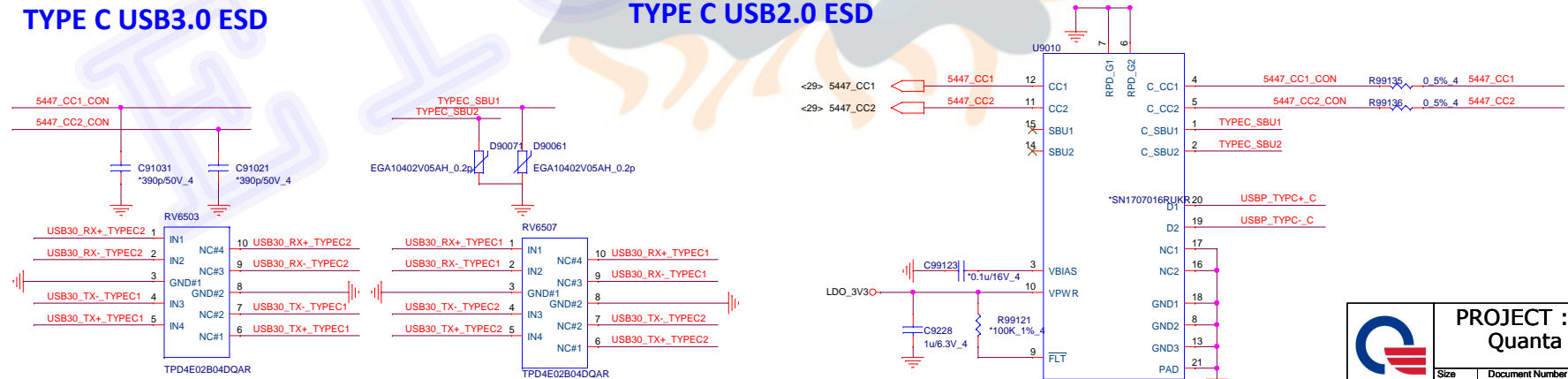
<4,26,29,32,33,37,38,39,40,41,42,43,45,46,47,48> +5VS5  
<4,12,13,15,29,32,33,34,35,38,39,40,41,45,48> +3VS5  
<4,10,11,12,13,14,15,17,18,22,25,26,27,28,29,31,32,33,34,35,42,45,46,47> +3V  
<29> +TYPEC\_VBUS

30



## TYPE C USB3.0 ESD

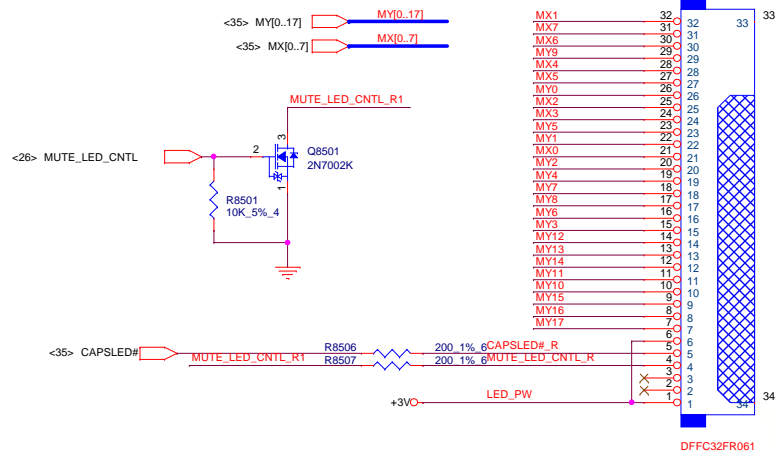
## TYPE C USB2.0 ESD



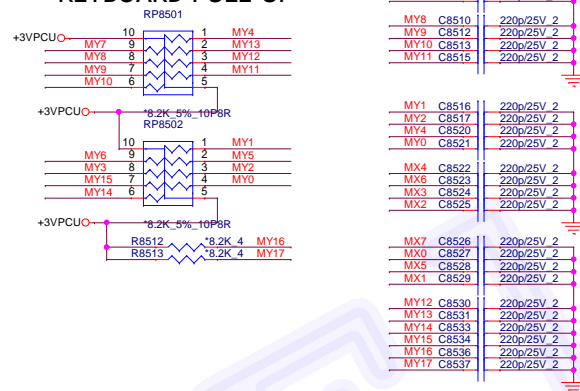
**PROJECT : G7BD**  
**Quanta Computer Inc.**

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Custom	USB SW/TYPE-C RT5447 & ESD	1.0
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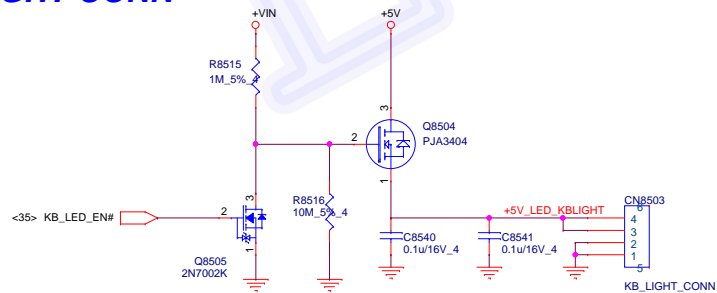
## KEYBOARD Con.



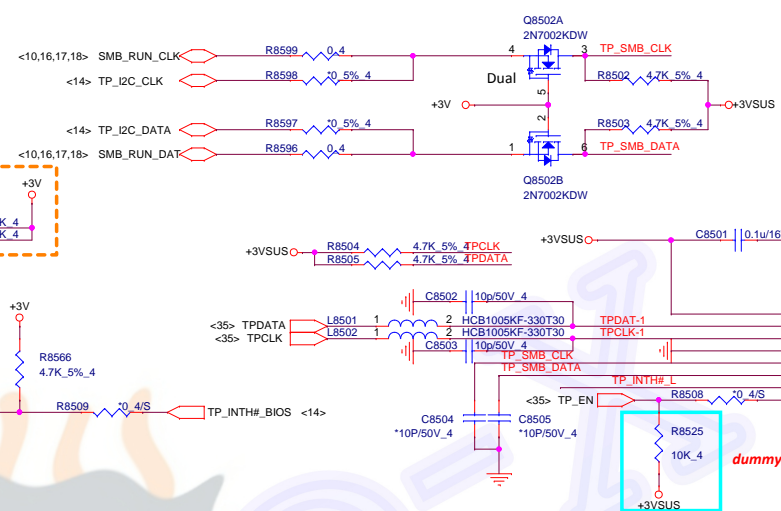
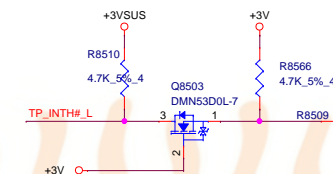
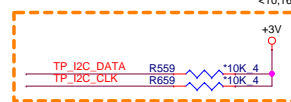
## KEYBOARD PULL-UP



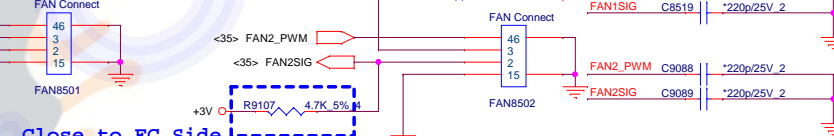
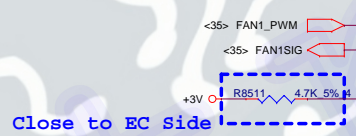
## KB LIGHT CONN



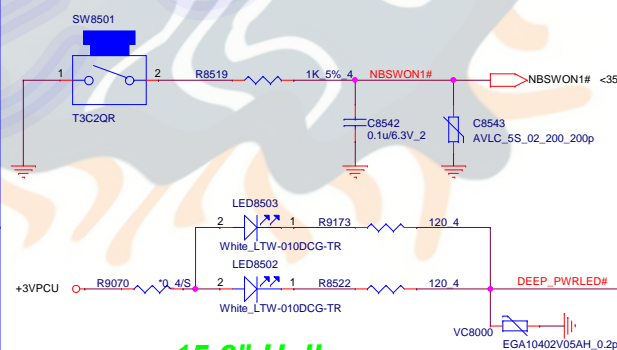
## Touch Pad



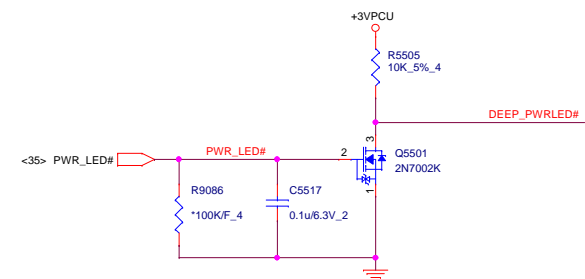
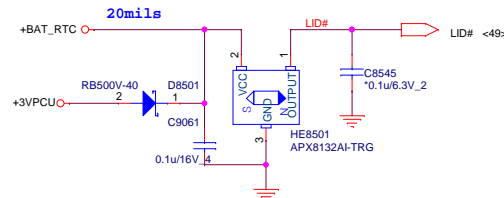
## FAN



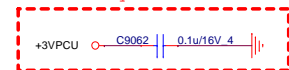
## PWR Button & LED & HALL IC



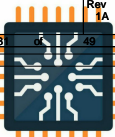
## 15.6" Hall sensor



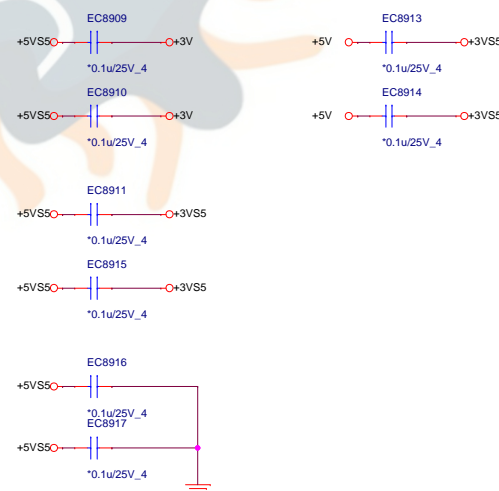
for EMI request



PROJECT : G7BD		
Quanta Computer Inc.		
Size	Custom	Rev
33 -- KB/TP/FAN		1A
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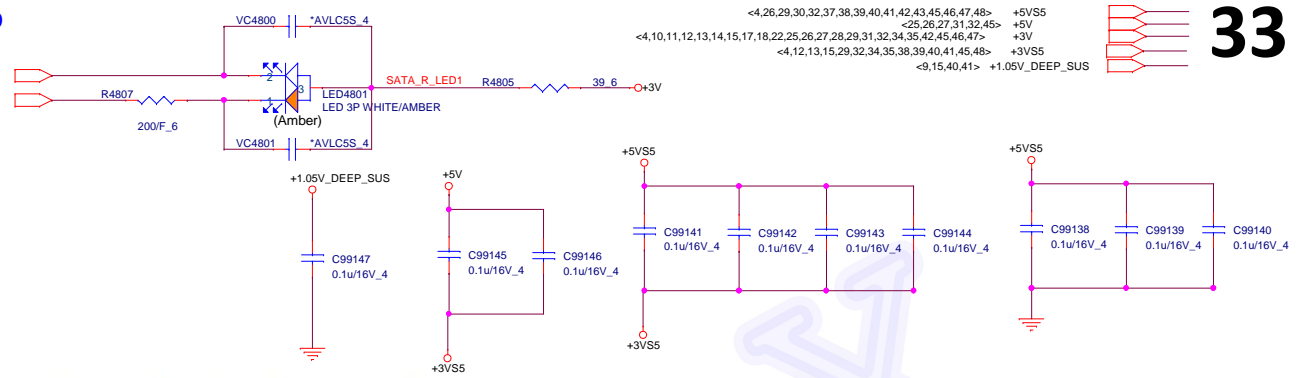
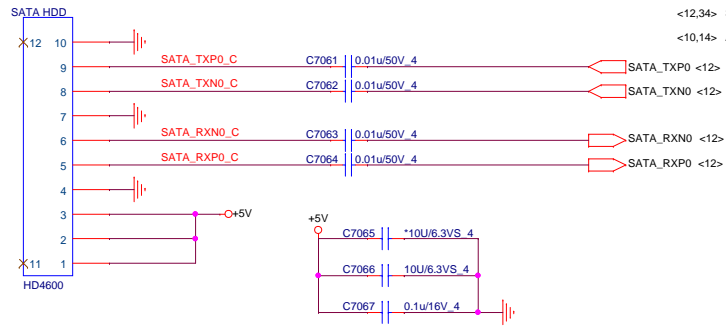
**change to FW 5.6 I**  
**PN:AL009665013**



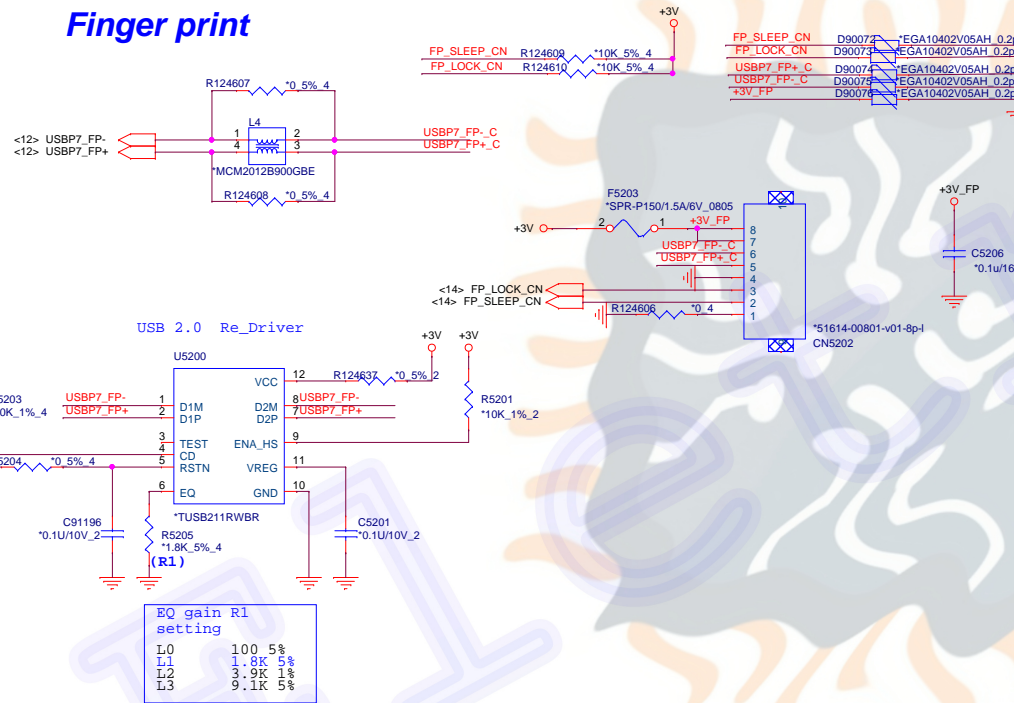


# SATA HDD & LED

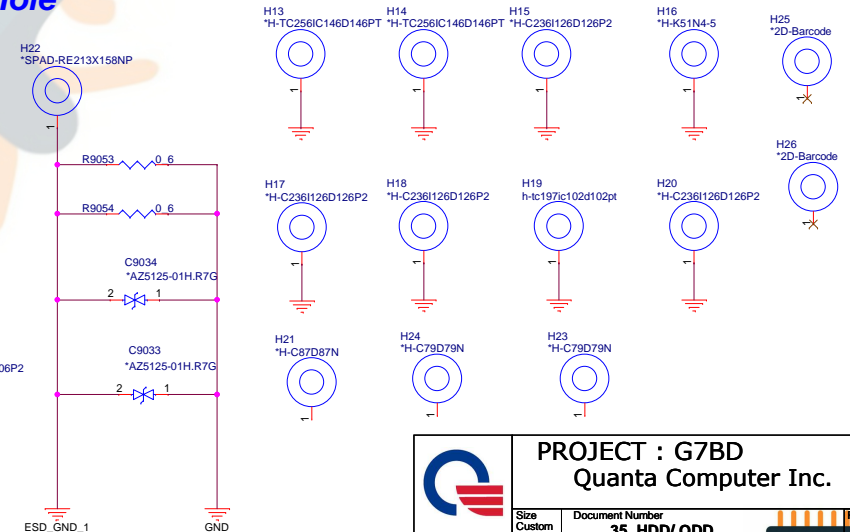
## SATA LED



## Finger print



## Hole

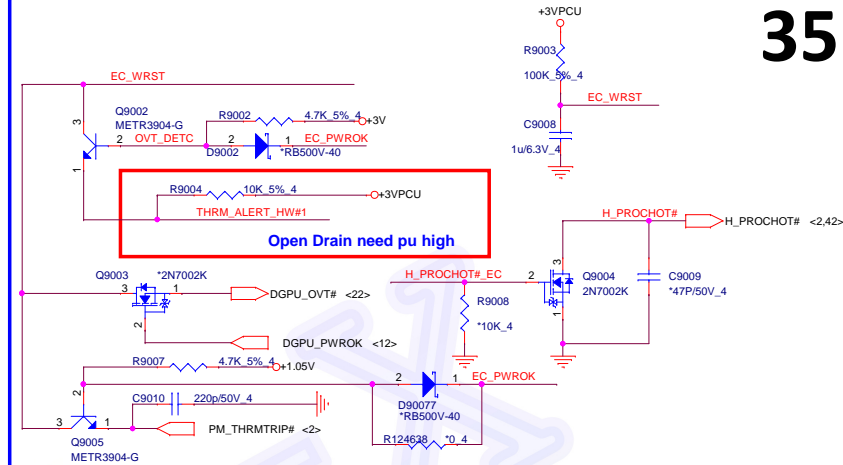
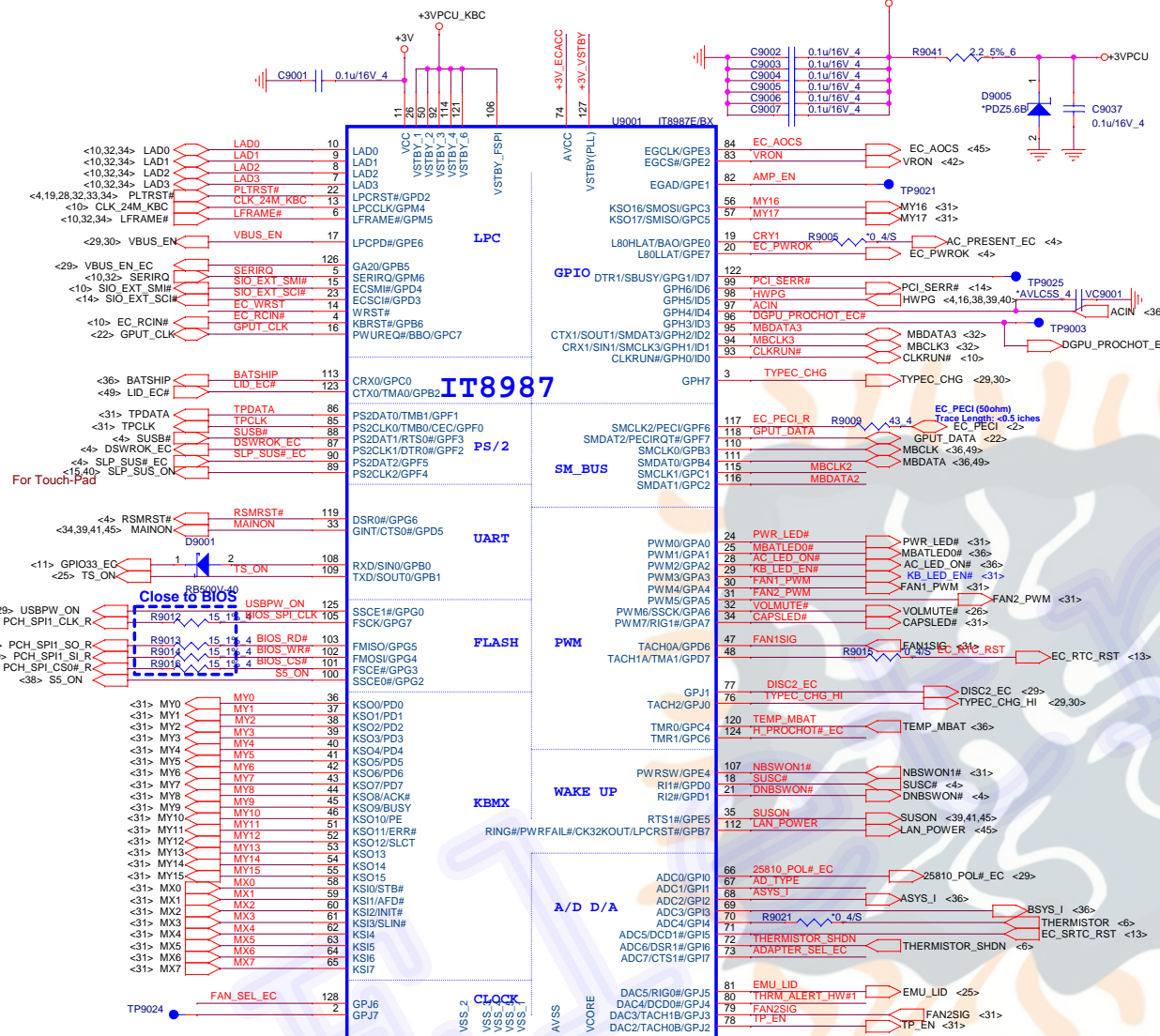


**PROJECT : G7BD**  
**Quanta Computer Inc.**

Size Custom Document Number **35 HDD/ ODD** Rev 00

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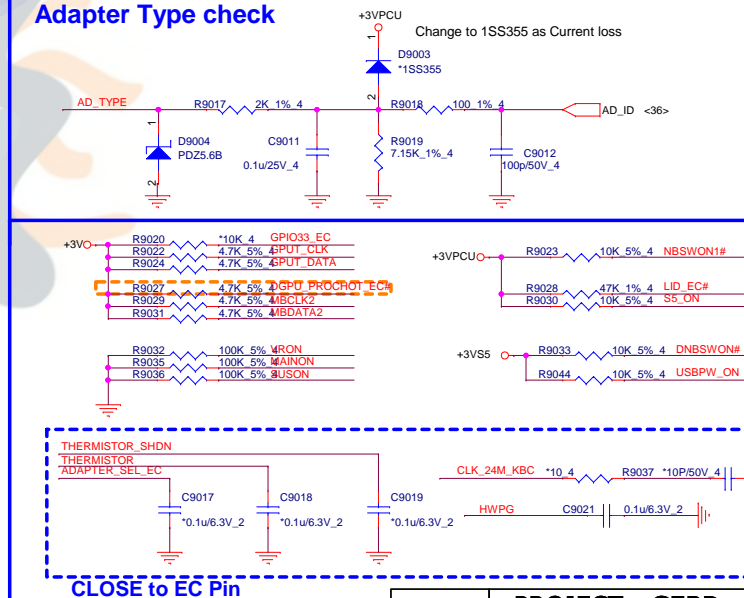




### Adapter select for EC

	Ra	Rb	ADAPTER_SEL_EC	BOM
200W	10K(CS31002FB26)	100K (CS41002FB28)	3V	
150W	10K(CS31002FB26)	100K (CS41002FB28)	3V	
120W	10K(CS31002FB26)	21.5K(CS32152FB09)	2.25V	
90W	10K(CS31002FB26)	8.25K(CS28252FB07)	1.5V	
65W	10K(CS31002FB26)	2.94K(CS22942FB01)	0.75V	DIS
45W	NC	10K(CS31002JB28)	0V	UMA

### Adapter Type check



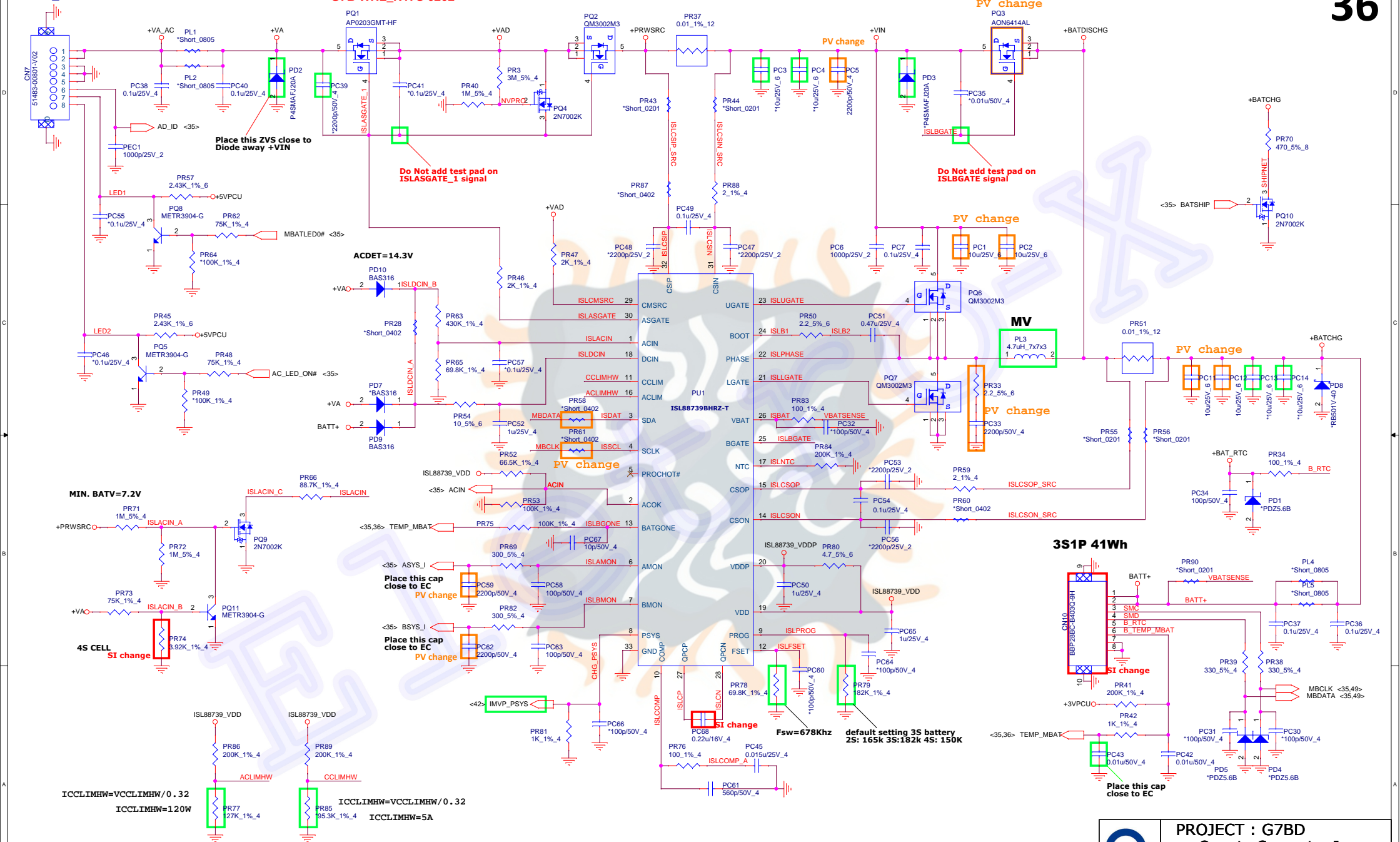
<4,10,11,12,13,14,15,17,18,22,25,26,27,28,29,31,32,33,34,42,45,46,47>  
 <4,12,13,15,29,32,33,34,38,39,40,41,45,48>  
 <6,13,31,34,36,38,49>

+3V  
 +3VS5  
 +3VPCU



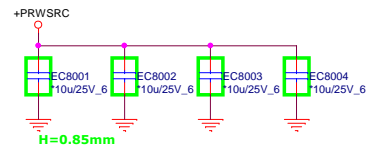
**DCIN CONN**

**G7B WHL N17S 0202**

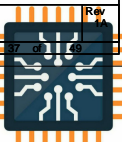
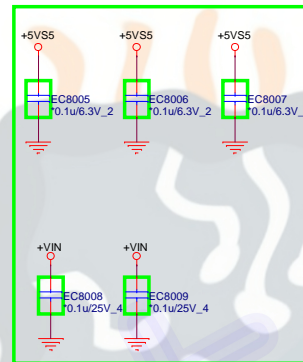




## Acoustic Solution

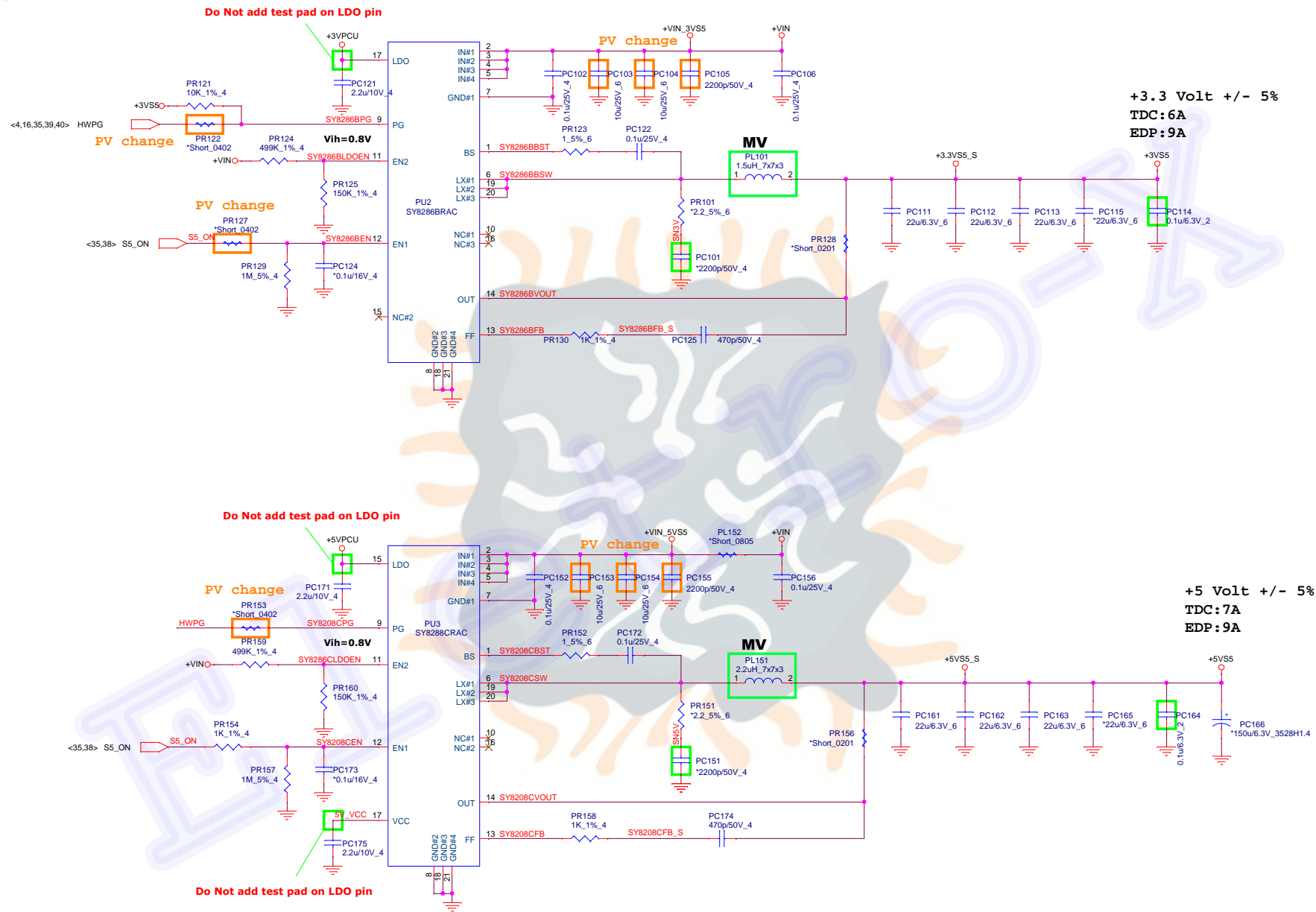



EMI suggestion to reserve

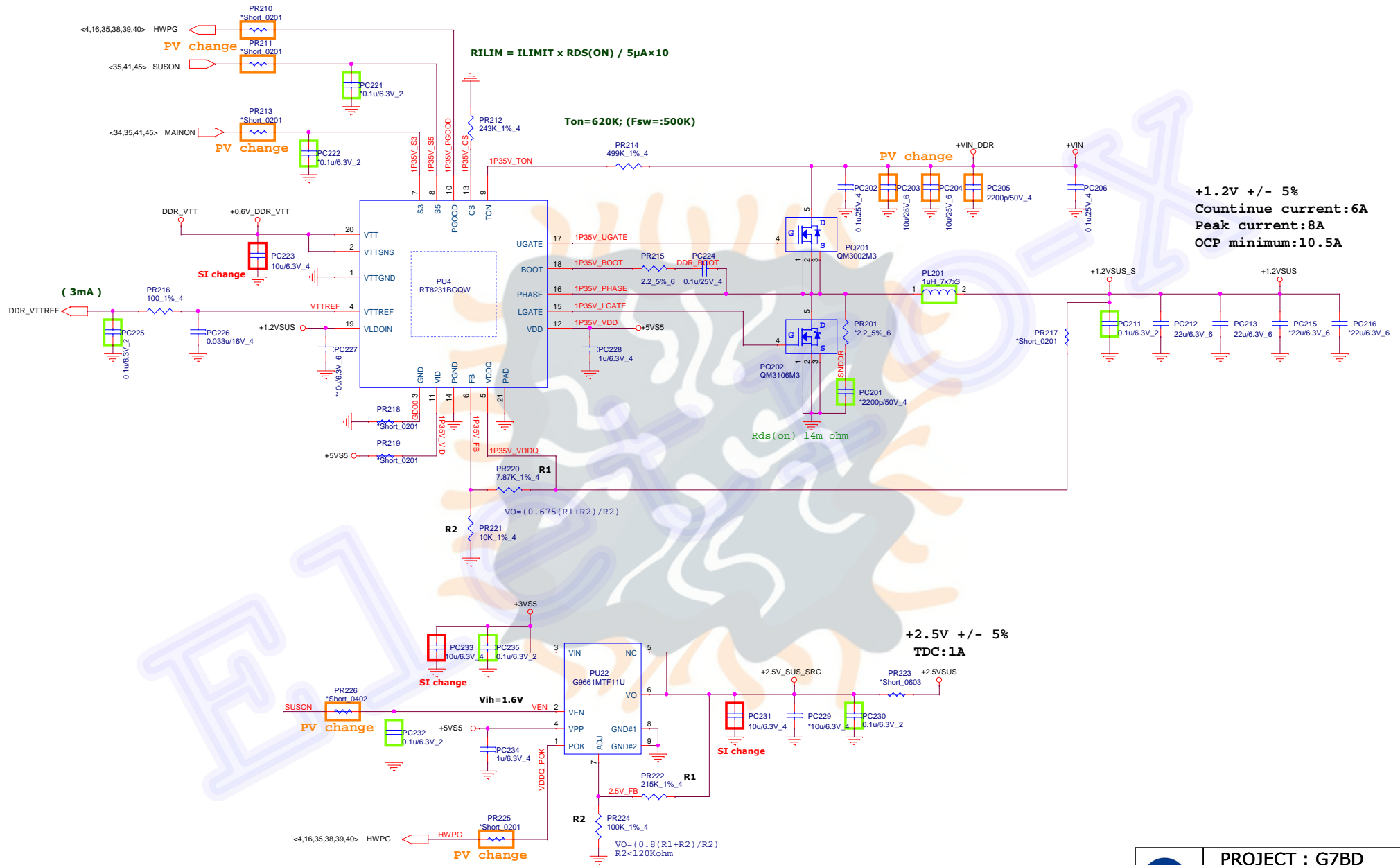


## DC/DC +3VS5/+5VS5

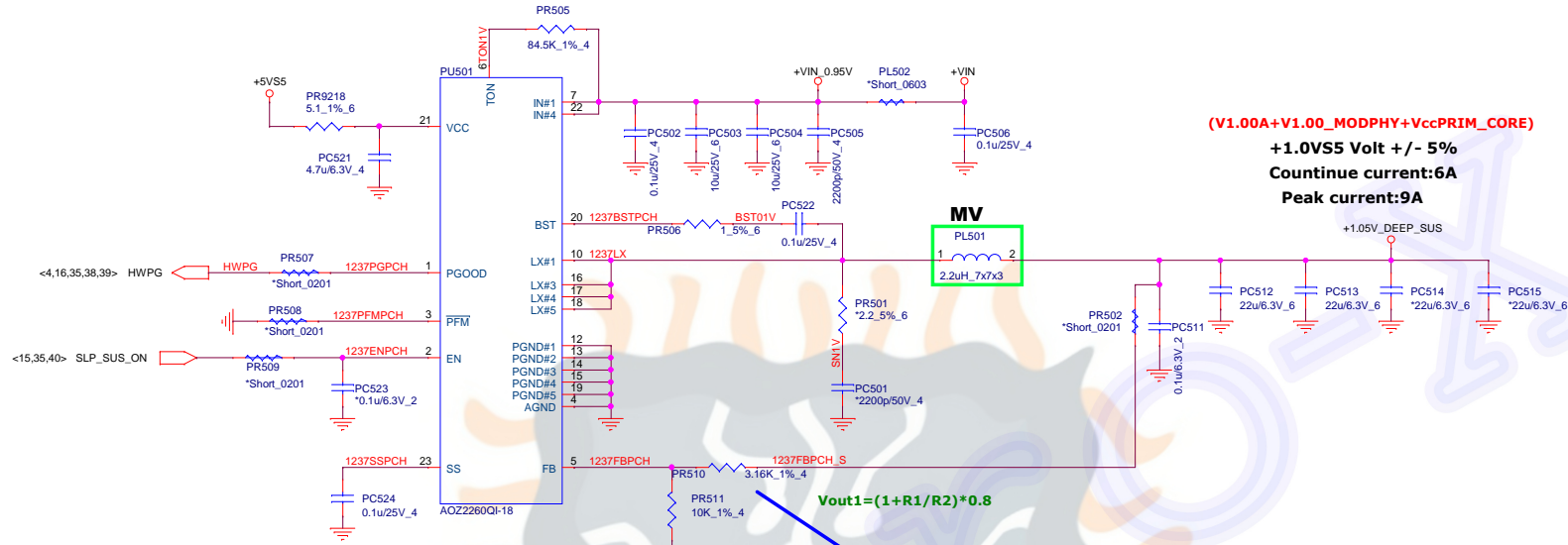
+VIN <25,31,36,37,39,40,43,44,46,47>  
 +3VS5 <4,12,13,15,29,32,33,34,35,39,40,41,45,48>  
 +5VS5 <4,26,29,30,32,33,37,39,40,41,42,43,45,46,47,48>  
 +3VPCU <6,13,31,34,35,36,49>  
 +5VPCU <28,34,36,45,48>



		PROJECT : G7BD Quanta Computer Inc.	
Size Custom	Document Number <b>+3/5VS5( SY8286B/SY8286BFS)</b>	Rev 1.0	
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+VIN <25,31,36,37,38,39,43,44,46,47>  
+3VS5 <4,12,13,15,29,32,33,34,35,38,39,41,45,48>  
+5VS5 <4,26,29,30,32,33,37,38,39,41,42,43,45,46,47,48>  
+1.05V\_DEEP\_SUS <9,15,33,41>  
+1.8V\_DEEP\_SUS <13,15,29,34,45,48>  
MAINON <34,35,39,41,45>  
+1.5V

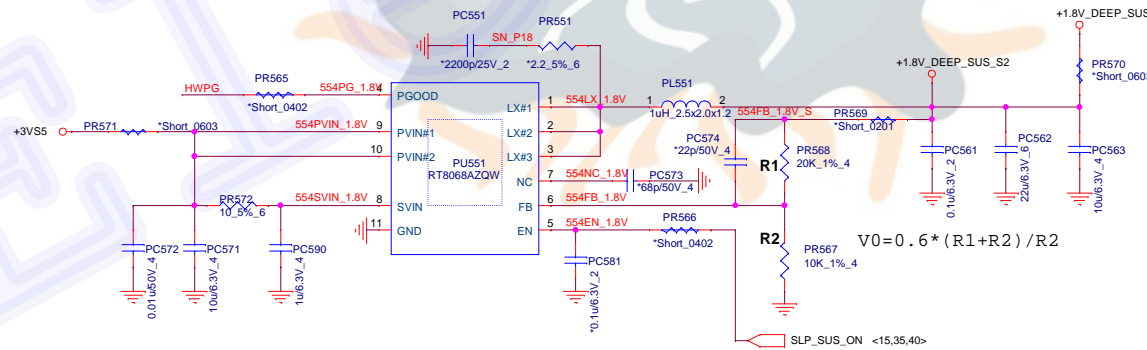


(V1.00A+V1.00\_MODPHY+VccPRIM\_CORE)  
+1.0VS5 Volt +/- 5%  
Countinue current:6A  
Peak current:9A


Vo	Rton
0.95V	82k
1V	84.5k
1.05V	95.3k
1.35V	113k
1.5V	127k

	1.91K	CS21912FB13	0.95V
SKL/KBL		CS22612FB15	1V
CNL/CFL/WHL	3.16K	CS23162FB04	1.05V

1.8VS5 +/- 3%  
TDC: 3A  
EDP: 4A



$$V0 = 0.6 * (R1 + R2) / R2$$



PROJECT : G7BD  
Quanta Computer Inc.

Size Custom

Document Number  
+1.0V/+1.8V\_DEEP\_SUS

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Rev

40



SKY/KBY-U22/U42/U23e  
KBY-G/WHL-U  
Vcc\_IO: 3.4A/1V  
Stuff PU601

## Stuff PU601 & merge 1V\_deep\_sus

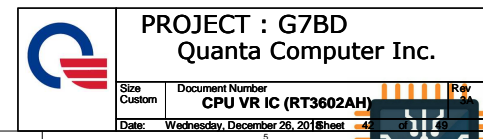
Unstuff PU603  
Unstuff PU601

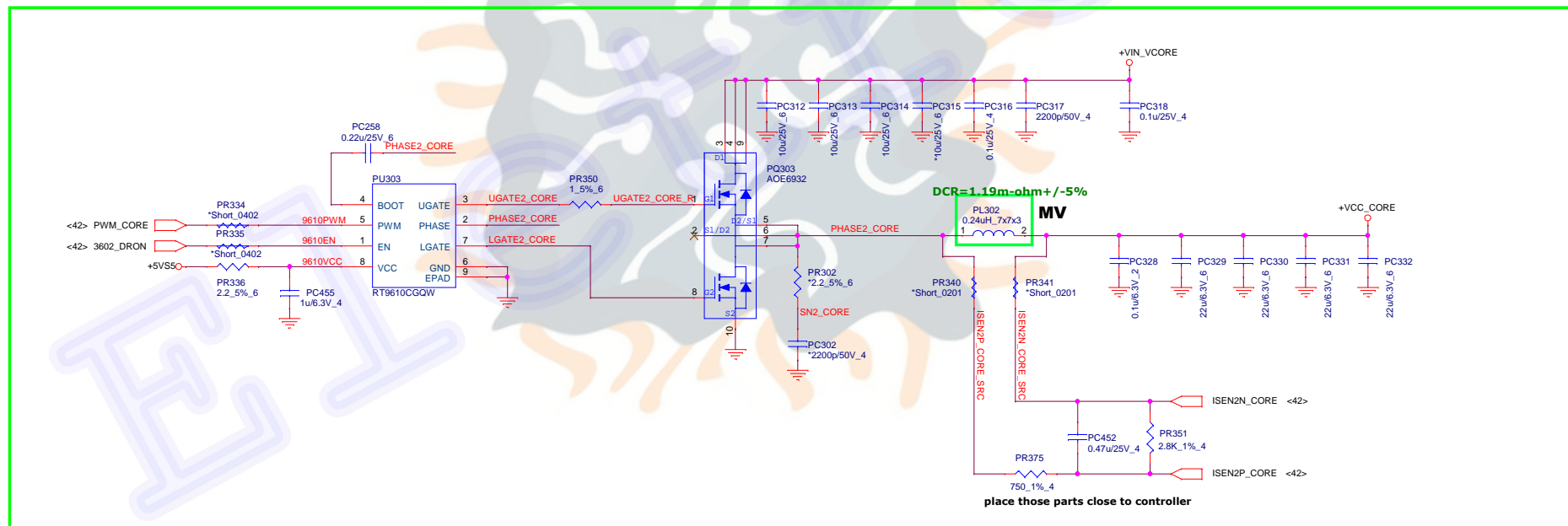
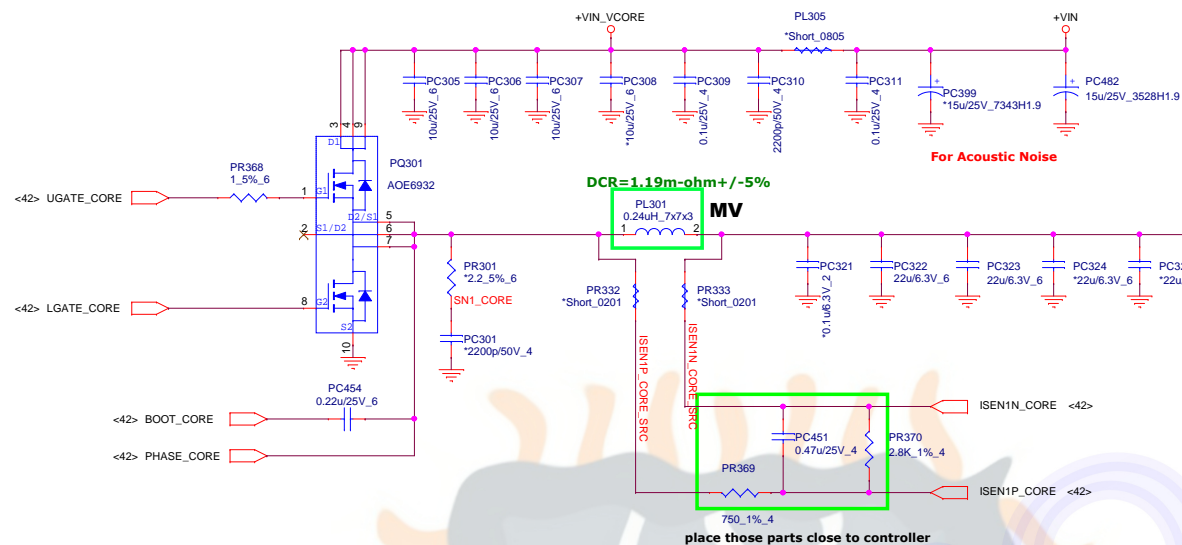
## Unstuff PU601

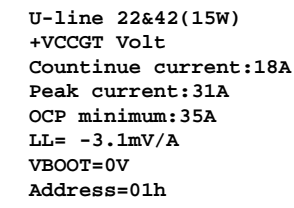
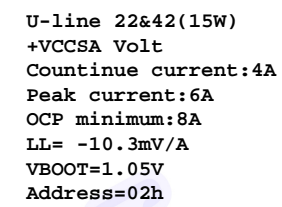
(Vcc\_ST+Vcc\_PLL)

**Imax:0.02A**

49

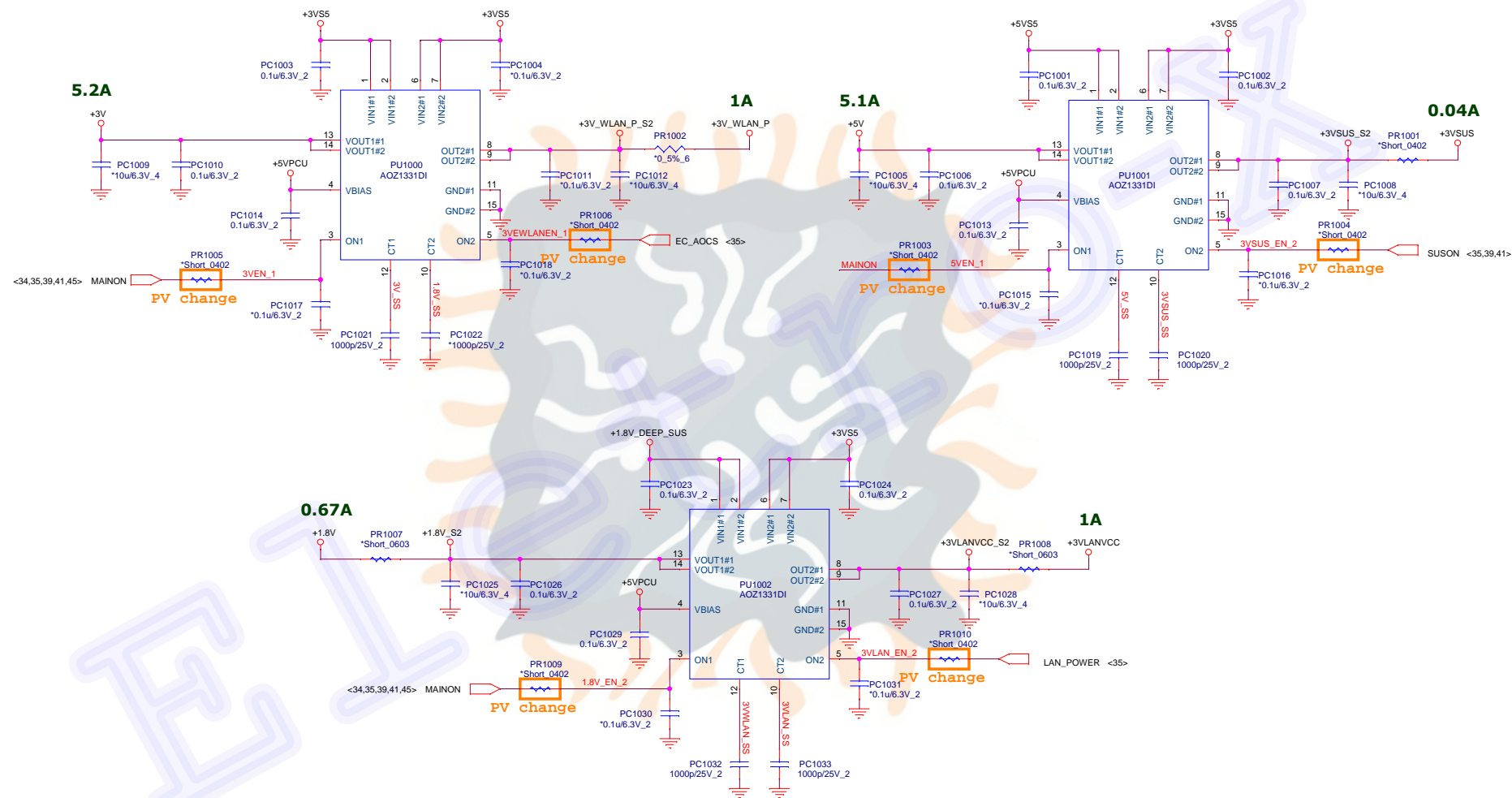






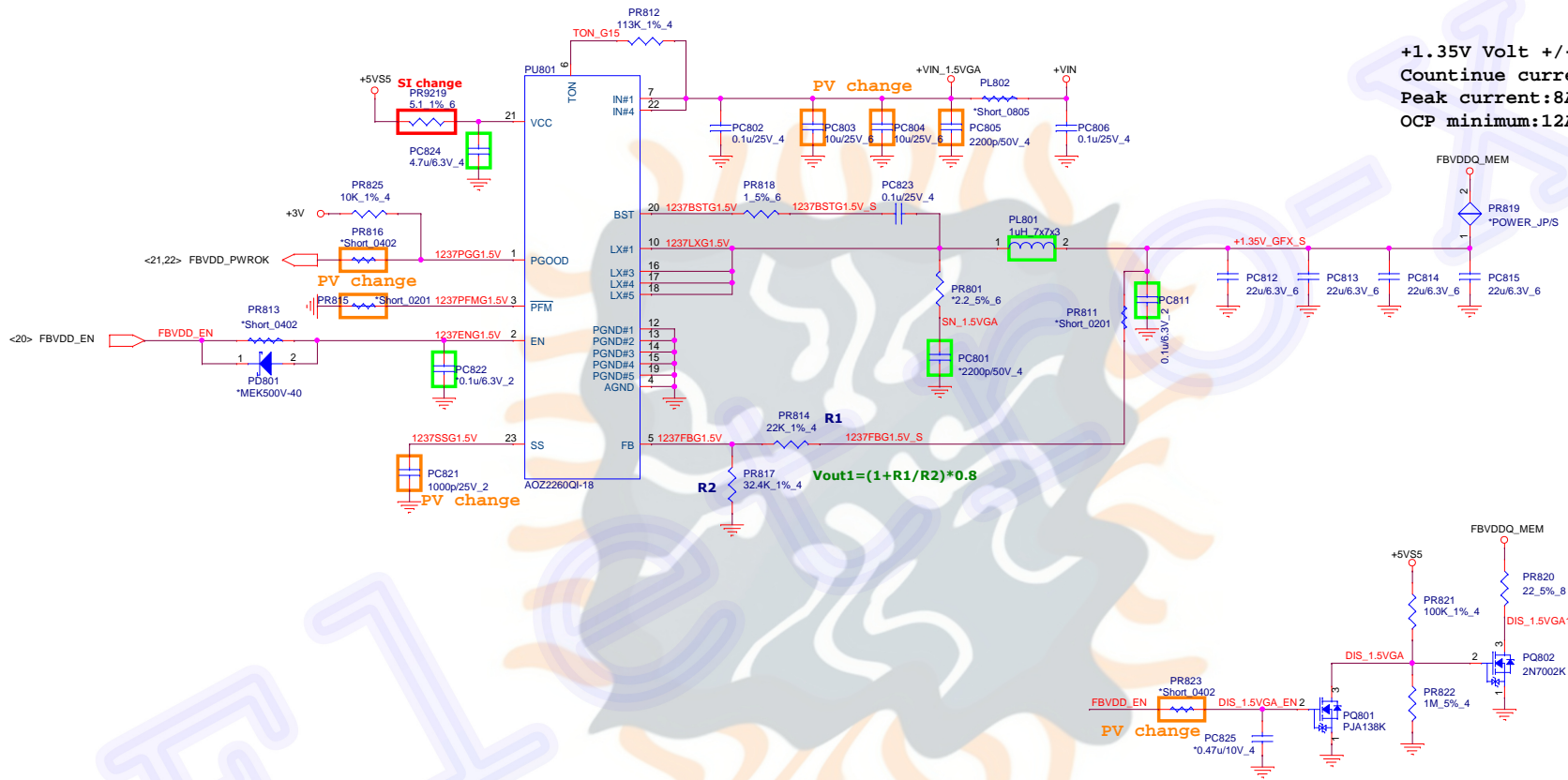
U22 & U42: VCCGT  
1\*330uF/9m+26\*22uF MLCC (total with EE)

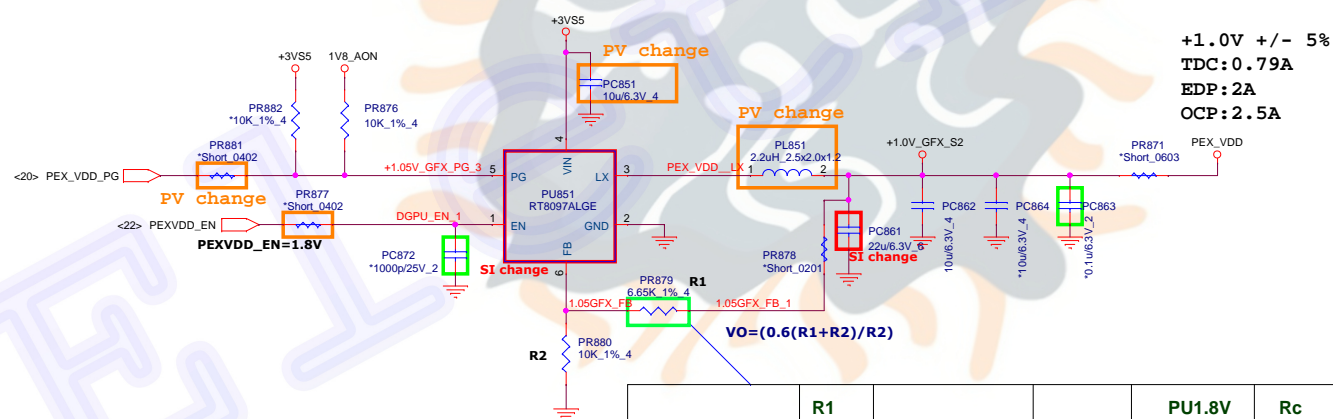
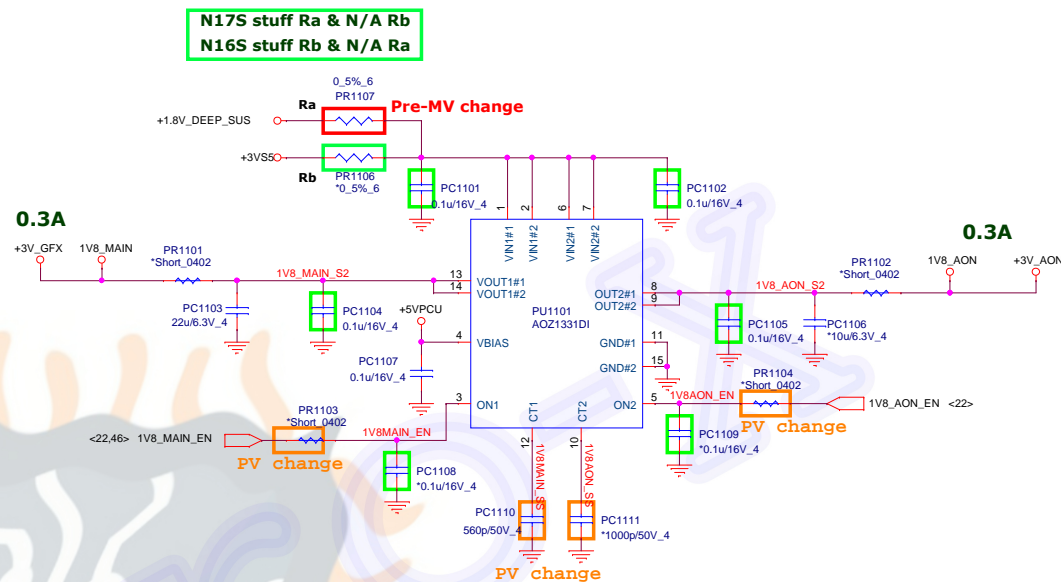
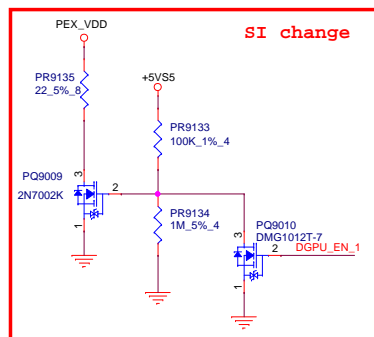






+VIN <25,31,36,37,38,39,40,43,44,46>  
+5VS5 <4,26,29,30,32,33,37,38,39,40,41,42,43,45,46,48>  
FBVDDQ\_MEM <20,21,23>





	R1			PU1.8V	Rc	Rd
N17P N17S	6.65K	CS26652FB06	1V	Unstuff	Unstuff	Stuff
N16S GTR	7.5K	CS27502FB11	1.05V	Unstuff	Stuff	Unstu

